

HOT CHIPS

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ADVANCE PROGRAM August 21-23, 2016

A Symposium on High-Performance Chips
Flint Center for the Performing Arts-Cupertino, CA

<http://www.hotchips.org>

HOTCHIPS brings together designers and architects of high-performance chips, software, and systems. The tutorial and presentation sessions focus on up-to-the-minute developments in leading-edge industrial designs and research projects.

Register Now: <https://www.123signup.com/register?id=nfkqk>

Sunday August 21	Tutorial 1: Using next generation memory technologies: DRAM and Beyond Memory technologies such as DRAM are rapidly changing from traditional interfaces and DRAM based devices to new interfaces, packages and device technologies. This tutorial will describe new technologies from industry leading memory vendors and show how they are used in new and emerging products and applications. Presenters include speakers from Micron, SK hynix, Samsung, Xilinx and more...	
	Tutorial 2: 3D depth for consumers: From Sensors to Applications 3D depth sensors are becoming increasingly ubiquitous, moving from robots and factories into cars and phones. Learn how sensor manufacturers, vision processing companies and application developers are enabling new depth - powered experiences for consumers. Presenters include speakers from PMD Tech, Inuitive, Movidius, Google, and more...	
Monday August 22	GPUs and HPC Processors	ARM Nvidia ARM
	Processing on the Go: Mobile Devices	NVIDIA
	<ul style="list-style-type: none"> • The New GPU Architecture and its Initial Implementation • Ultra-Performance Pascal GPU and NVLink Interconnect • ARMv8 - A Next-Generation Vector Architecture for HPC 	
	<ul style="list-style-type: none"> • NVIDIA Tegra - Next System-on-Chip • Helio X20: The First Tri-Cluster Deca-Core Mobile Application Processor SoC with CorePilot 3 Technology for High-Performance and Power-Efficiency • Samsung's Exynos-M1 CPU 	Mediatek Samsung
	Keynote A: Augmented Reality Ilan Spillinger, CVP HoloLens Technology and Silicon	Microsoft
Tuesday August 23	Energy-Efficient Computing: Low-Power SoCs	Intel Psikick
	Vision and Image Processing	Deepphi and Tsinghua Ceva Cadence
	<ul style="list-style-type: none"> • Design and Development of a an Ultra-Low Power x86 MCU Class SoCs • A Sub-GHz Wireless SoC for Batteryless IoT Applications 	
	<ul style="list-style-type: none"> • Model to FPGA: Software-Hardware Co-Design for Efficient Neural Network Acceleration • The Path to Embedded Vision and AI using a Low-Power Vision DSP • High-Performance DSP for Vision, Imaging and Neural Networks 	
	Interconnects: Microns to Kilometers	TSMC InPhi Intel
Tuesday August 23	<ul style="list-style-type: none"> • A 16nm 256-bit Wide 89.6GByte/s Total Bandwidth In-Package Interconnect with 0.3V Swing and 0.062pJ/bit Power in InFO Package • 100Gbit/s, 120km, PAM 4 Based Switch to Switch, Layer 2 Silicon Photonics based Optical Interconnects for Datacenters • Intel Omni-Path 4.8 Tbps Switch ASIC and Platform 	
	Emerging Embedded	Sentons Invisage Levant
	<ul style="list-style-type: none"> • A "Zero-displacement" Active Ultrasonic Force Sensor for Mobile Applications • Quantum Dot-Based Imagers for Multispectral Cameras and Sensors • Building the World's First Super Active Suspension System 	
	Keynote B: Are We There Yet? Silicon in Self-Driving Cars Daniel Rosenband, Compute Lead,	Google
	Many-Core Chips	Princeton University UC Davis
	<ul style="list-style-type: none"> • Piton: A 25-Core Academic Many-Core Processor • KiloCore: A 32 nm 1000-Processor Array 	
Tuesday August 23	Dealing with Big Data	Movidius Oracle Baidu
	<ul style="list-style-type: none"> • Embedded Deep Neural Networks: "The Cost of Everything and the Value of Nothing" • Software in Silicon in the Oracle SPARC M7 processor • SDA: Software-Defined Accelerator for General-Purpose Distributed Big Data Analysis System 	
	High-Performance Processors	Intel IBM AMD
	<ul style="list-style-type: none"> • Inside 6th-generation Intel Core Code-Named Skylake: New Microarchitecture and Power Management • POWER9: Processor for the Cognitive Era • A New, High-Performance x86 Core Design from AMD 	



A Symposium of the Technical Committee on Microprocessors and Microcomputers
of the IEEE Computer Society and the Solid-State Circuits Society