

# IEEE GRID *.pdf*

OCTOBER 2003

**It's Back to School time  
in the Valley. David Fong's  
SCV K-12 Education Committee  
needs volunteers!**

*See page 3*



# IEEE President Elections VOTE NOW



You have received your annual election ballot in the mail. Please do your duty as an IEEE member and vote. You have a chance to vote for President Elect 2004 becoming President in 2005. Two outstanding candidates are running; Cleon Anderson from our Region 6 and Mike Lightner from Region 5. The President of IEEE shapes your organization for years to come, so this is a very important choice for you to make.

Region 6 consists of the 12 Western states of the US and is the largest region in IEEE with over 60,000 members. It also has the largest Section in the world (Santa Clara Valley Section) with over 20,000 members. It is time for us to have a voice at the top in how Region 6 and the other regions should be run. Region 6 has not had a President of IEEE since Carleton Bayless in 1990. This is too long without representation in this key position.

We want to set another record and have a higher percentage of people voting from Region 6 than from any other region in the World. For further information go to <http://www.cleonanderson.com>

# IEEE GRID.pdf

October 2003 • Volume 50 • Number 10

## IEEE-SFBAC 2003

*Chairman*

**Mahbub R. Khan, PhD**

*Finance Chair*

**Kirti S. Shah, PE**

*Editorial Board Chair*

**Ray Holstead, PE**

*OEB Director*

**Douglas B. Snow, PE**

*SF Director*

**James B. Lekas**

*SCV Director*

**Jonathan B. David**

*ECI Directors*

**James Lamb**

**James Hungerford**

**Bernie Siegal**

*SFBAC Manager*

**Marilyn Turner**

IEEE-SFBAC

540 University Avenue  
Suite 150

Palo Alto, CA 94301

Tel: 650 327-6622

Fax: 650 321-9692

E: [ma.turner@ieee.org](mailto:ma.turner@ieee.org)

IEEE Grid is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE Grid are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities on a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

IEEE Grid is published as an Online Edition residing at [www.ieee-sfbac.org](http://www.ieee-sfbac.org) and in this handy printable pdf edition, sent by email each month to more than 24,000 Bay Area members.



Editor: Doug Davolt

IEEE GRID

278 W. 42nd Avenue

San Mateo CA 94403

Tel: 650 571-0119\

Fax: 650 571-5585

E: [d.davolt@ieee.org](mailto:d.davolt@ieee.org)

[www.ieee-sfbac.org](http://www.ieee-sfbac.org)

## From the editor . . .



### It's Back to School in the Valley!

IEEE Santa Clara Valley K-12 Education Committee needs volunteers to assist with its 2003-2004 program. Specifically they need help in these areas.

- Tutoring and mentoring
- Teaching teachers
- Funding
- Lego Robotics
- Science Fair judging
- Laser optics

If you can help out, please call David Fong at 510 687-4507 or email him at [daffy@ieee.org](mailto:daffy@ieee.org).

Take a look at the Web site at

[www.ewh.ieee.org/r6/scv/k-12/index.html](http://www.ewh.ieee.org/r6/scv/k-12/index.html)

for more details.

—Ed.

NOTE: IEEE GRID.pdf is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and interactive calendar for the latest information.

Subject: **Real time digital pro audio transport and control over Ethernet**

Speaker: Barani Subbiah (NetworkSound Inc.)

Time: Refreshments at 7:00 p.m., presentation at 7:30

Place: Cogswell College, Dragoon's Den, 1175 Bordeaux Dr. Sunnyvale

RSVP: Not required

## Real-time pro audio transport and control over Ethernet

Ethernet is established as the predominant standard in the networking industry and has been used in pro audio industry for some time. NetworkSound, Inc., a silicon valley spinoff, is poised to deliver digital transport and control solutions over Ethernet for the pro audio market. The company's vision is to enable a networked pro audio system in which all audio devices connected to the network are able to transport, control, modify, and add effects to digital audio carried over the network. The cost saving on "snake" is an added bonus to use a digital Ethernet based solution.

Barani Subbiah will present this technology at the October 2 meeting of the Santa Clara Valley Signal Processing Society in conjunction with the San Francisco Audio Engineering Society. There will be demo of Digital Guitar to showcase NetworkSound technology.

Barani Subbiah is the founder and CEO of NetworkSound, Inc. He has over 18 years of experience in computer networking and the wireless industry. Most recently, he was with 3Com as director of the Technology Development Center and later managed the Pro audio business.

He has negotiated many licensing and business deals for 3Com with various customers. He has over 20 published papers in journals, magazines, and conferences, and has 34 patents either issued or pending. He was a founding member and visiting research scholar with Stanford Networking Research Center and an invited speaker at many events.

**WEDNESDAY OCTOBER 8**

SCV Components, Packaging & Manufacturing Technology

Subject: **Flexible Automation - Going Where Human Eyes and Fingers Cannot Go**

Speaker: Charlie Duncheon (Adept Technology, Inc)

Time: Seated dinner at 6:30 (\$25 if reserved before October 4; \$30 after and at door; vegetarian available) presentation (no cost) at 7:30

Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expressway and Great America Parkway), Sunnyvale, (800 888-3899)

RSVP: Register and prepay for dinner (\$25) in one step from your PayPal account or Credit Card - Allen Earman - cpmt.scv.treas@ieee.org Please reserve for "presentation-only" if not attending the dinner

Web: <http://cpmt.org/scv/meetings/cpmt0310.html>

**Flexible Automation -  
Going Where Human  
Eyes and Fingers  
Cannot Go**

Charlie Duncheon will be the featured speaker at the October 8 meeting of the SCV CPMT chapter. His presentation will focus on new fields in automation where justification is not based on labor savings but rather production yields and quality. Specific applications in semiconductor processing, both in the front end and the back end, will be presented. Sub-micron assembly applications will also be presented in the fiber optic components market. Other automation tools like 3D simulation and vision guided flexible feeding will be presented. Lastly, automation economics will be discussed as it relates to justification in low cost labor markets like China.

Charles S. (Charlie) Duncheon is executive vice president for Adept Technology Inc. Besides being responsible for global sales, marketing and customer service at Adept, he is responsible for the precision assembly and semiconductor solutions division. His past positions at Adept include senior vice president of worldwide sales, marketing and customer service, as well as business development.

During his tenure, Duncheon has been instrumental in leading the company to become a market share leader in the small parts handling, assembly, and robot motion controller markets. He drove sales and marketing expansion into international markets and developed key relationships with OEMs, integrators, and other channel partners. He became CEO of Fastfactory In 2000 but returned to Adept when Fastfactory was Integrated Into Adept in 2001.

Prior to Adept, Duncheon served as vice president of sales and marketing for FARED Robot systems, a systems integrator. He also held several engineering and manufacturing positions at Monsanto Company.

Duncheon is a member of the board of directors of the Robotic Industries Association (RIA) having served as president from 1997 to 1999. In addition, he has served on the Academic Advisory Board for Purdue University School of Engineering Technology and the Advisory Board of the Arlington Robotics Research Institute of the University of Texas.

**WEDNESDAY OCTOBER 8**

SCV Communications Society

Subject: **Mobile Broadband Wide Area Access Technologies**

Speaker: Dr. Marc Goldberg (ArrayComm)

Time: pizza and sodas at 6:30 p.m.,  
presentation at 7:00

Fee: \$1 donation to partially cover food cost

Place: National Semiconductor Credit Union,  
Bldg. 31, 955 Kifer Rd., Sunnyvale

RSVP: [rsvp@comsocscv.org](mailto:rsvp@comsocscv.org)

Web: <http://www.comsocscv.org>

## Mobile Broadband Wide Area Access Technologies

Wireless system designs trade off coverage, spectral efficiency, mobility performance and a host of other factors in support of a particular service vision. Marc Goldberg will discuss this technology at the October 8 meeting of the Santa Clara Valley Communications society.

In his talk, Goldberg discusses the design and performance of the iBurst system. iBurst has been developed to provide mobile wide-area broadband services with economics that permit mass-market pricing. Overviews of the iBurst network and air interface architectures will be presented, including an introduction to adaptive antennas. Results from the field and the IEEE 802.20 standardization process will also be provided.

Marc Goldberg has been at ArrayComm since the company's inception in 1992. In addition to his work on architectures and protocols for wireless data systems, he has played a lead role in the development of ArrayComm's spatial processing technology for cellular voice and data systems. Marc's group is responsible for core technology development at ArrayComm, and for the company's regulatory and standards efforts.

Marc is an adviser to the Federal Communication Commission's Spectrum Policy Task Force, and has delivered many invited tutorials to the FCC and other national and international regulatory agencies on the topics of adaptive antennas, spectral efficiency and spectrum policy. Scientific American recently honored Marc as 2002 Research Leader in Communications in its first annual "Scientific American 50" awards for his pioneering work on adaptive antenna technology.

Prior to ArrayComm, Marc's experience includes a staff position at MIT Lincoln Laboratory and a research position at Stanford University. He holds patents relating to spatial processing methods for wireless voice and packet data systems, and he has published a number of technical papers in the areas of communications and signal processing. Marc holds a PhD in electrical engineering from Stanford University, an MSEE from the University of Washington, and a BSE. (EE) from Princeton University.

**TUESDAY OCTOBER 14**

SCV CPMT

Subject: **Short Course - Collaborative  
Negotiating for Engineers**

Instructor: Ed Levine

Time: 8:30 a.m. - 4:30 p.m.

Place: Philips Semiconductors, 1150 Ringwood  
Court, San Jose

Cost: \$400 (\$325 for IEEE Member/Corporate  
Training Partner)

Register: [www.cpmt.org/scv/](http://www.cpmt.org/scv/) or 408-866-6172

## Collaborative Negotiating for Engineers

With techniques from the Harvard Negotiating Project, participants in this course will learn how to shift from win-lose to win-win strategies that enable both parties to come away from the table with more than either of them had hoped for. Through a series of classroom negotiations, participants discover practical approaches for countering the tactics of the 'hard' negotiator and keeping negotiations from slipping into rights or power-based conflicts. Learn a systematic, four-stage process of interests, options, alternatives, and credible criteria that increases both your negotiating skill and confidence.

Defining the boundary conditions for any successful negotiation, applying the three levels of listening that are key to resolving core issues, and the ability to anchor a negotiation within the zone of agreement provide participants with the essential skills to reach a mutually satisfying agreement.

You'll learn to: Identify Collaborative vs. Aggressive Styles; Use the Collaborative Negotiating Model; Handle the "Hard" Negotiator; Analyze Interests, Rights & Power; Create Options from Interests; Evaluate Priority Problems; Use the Impact of Objective Criteria; Use Approaches to the Zero-Sum Game; Explore Trust, Threats & Competition; Understand the Bargaining Zone; Avoid Making Common Mistakes; Understand Post-Settlement Settlements; and Make and Implement Agreements.

Ed Levine has been a training consultant since 1991. Previous to that, he was a sales and branch manager for ComputerLand Corporation. He went on to found a start-up company selling Computer Aided Design (CAD) systems to engineers in the Bay Area. Ed negotiated the sale of his business to a multi-national competitor after years of exponential growth. The training and the consulting side of his CAD business were what Ed always enjoyed most. As a result, Ed has been involved in the training and consulting field since 1992. He has taught "Collaborative Negotiating" many times for the IEEE.

**WEDNESDAY OCTOBER 15**

SCV Engineering in Medicine & Biology Society

Subject: **A Novel System for Cardiac Surgical Ablation**

Speaker: Michael Nasab (Circuit Mentor) and  
Eric K.Y. Chan (CARDIMA, Inc.)

Time: Dinner at 6:00 pm., presentation at 7:30

Place: Dinner in the Stanford Hospital Cafeteria,  
presentation in Room M114 of the  
Stanford Medical School

RSVP: Not required

## A Novel System for Cardiac Surgical Ablation

The CARDIMA INTELLITEMP® is a radiofrequency (RF) Energy Management Device that takes as input the RF energy from a commercially available RF generator such as a Valleylab electrosurgical unit, and channels it through eight ablation electrodes on the Surgical Probe.

The deflectable electrode section permits excellent electrode-tissue contact, resulting in efficient RF-coupling to form linear lesions. Thermocouples situated on the probe provide temperature feedback that regulates energy delivery to the electrodes. These electrodes emit at high current densities, ensuring creation of deep lesions with minimal power requirements. The resulting cardiac lesions replicate those of the highly successful surgical Maze procedure for the treatment of atrial fibrillation (AF).

The first procedure with the Surgical Ablation System was performed in August at the prestigious Lenox Hill Hospital in New York. In the aftermath of the procedure to treat a patient with a long history of chronic AF, Dr. Didier Loulmet, who heads up the Lenox Hill Hospital Atrial Fibrillation Program, commented that the *“unique technology behind the CARDIMA Ablation System proved to be a critical and powerful tool for this especially difficult case. The ease of use, the power, and the depth of penetration given the small size of the catheter is impressive.”*

Two speakers, Michael Nasab, principal of Circuit Mentor, and Eric K.Y. Chan, VP of product development for CARDIMA, Inc., will discuss this new product at the October 15 meeting of the Santa Clara Valley Engineering in Medicine & Biology Society. Their talk will discuss the functionality of the ablation system as well as include narratives of ‘real world’ open heart surgery experiences.

Michael Nasab is the principal of Circuit Mentor, an electronics consulting business based in Boulder Creek, CA. He received his engineering degrees from international as well as U.S. institutions. He was the R&D project manager and primary engineer of the INTELLITEMP® Energy Management Device at CARDIMA. His expertise is in R&D and product development in the fields of electromagnetics, power supply design, **LabVIEW** instrumentation development and system integration. He has held several engineering management and technical positions in Silicon Valley since 1986.

Eric Chan is VP of product development at CARDIMA, Inc. in Fremont, CA. He received his BSEE from Purdue University, MSE & PhD in BME from Univ. of Texas at Austin. He served as a past co-chairman of the Central Texas IEEE-EMBS. He has spent the last 12 years in the development of many commercially released medical products in the cardiology and cardiac electrophysiology (EP) field. He was recently elected a Fellow of the European Society of Cardiology.

## **UNIVERSITY OF CALIFORNIA, SANTA CRUZ**

### **Information Systems and Technology Management**

### **Assistant Professor**

The Information Systems and Technology Management Program at the University of California, Santa Cruz invites applications for a tenure track (Assistant Professor) faculty position. Due to the multidisciplinary nature of this program, we seek outstanding applicants with diverse backgrounds, and a combination of undergraduate and graduate degrees in business/economics and engineering/computer science is suggested. UCSC is the University of California campus closest to "Silicon Valley," and we have many ties with local industry, in research, startups, and consulting.

The emphasis of the program is systems at the boundary between technology and business, including but not limited to IT Management, e-business, supply chain management, multi-agent systems, mechanism design; stochastic optimization in enterprise management, financial engineering, new product development, knowledge management, data warehousing and data mining; decision support systems, network management; Internet and intranet tools; distance learning; computer-based process reengineering and the competitive use of information systems.

Applicants should submit a CV, a statement of research plans and teaching interests, and copies or URLs of selected reprints. Applicants should ensure that at least **three** confidential letters of recommendation are sent directly. Screening will begin with applications received by **December 1, 2003** or earlier and continue during academic year 2003-04; to ensure full consideration, applications must arrive by the deadline. Early applications are encouraged. **We strongly encourage electronic submission of your materials.** Directions are provided at <http://www.soe.ucsc.edu/jobs/>. All letters will be treated as confidential documents; please direct your references to UCSC's confidentiality statement at <http://www2.ucsc.edu/ahr/policies/confstm.htm>). Alternatively, application materials may be mailed to: Information Systems and Technology Management Search Committee, Baskin School of Engineering, 1156 High Street, University of California, Santa Cruz, CA 95064. For further details about the Baskin School of Engineering at UCSC, see <http://www.soe.ucsc.edu/>. Please indicate clearly that materials are for position #587.

***UCSC IS AN EEO/AA/IRCA Employer.***

**THURSDAY OCTOBER 16**

SCV Solid State Circuits Society

Subject: **Lossless Feedback Amplifier Design**

Speaker: Mr. George Vendelin (Consultant)

Time: Refreshments at 6:30 p.m.,  
presentation at 7:00

Place: Cadence Design Systems, Bldg. 5,  
2655 Seely Ave., San Jose

RSVP: [ssc\\_scv\\_rsvp@yahoogroups.com](mailto:ssc_scv_rsvp@yahoogroups.com) -  
for email reminder subscribe to  
[ssc-chpt-scv@majordomo.ieee.org](mailto:ssc-chpt-scv@majordomo.ieee.org)

## Lossless Feedback Amplifier Design

As more customer demand, activity and resources become available for designing RF circuits as part of a system on a chip it will become necessary to include some microwave theory in the ASIC designers knowledge base.

We are indeed fortunate to have George Vendelin available at the October 16 meeting of the Santa clara Valley Solid State Circuit Society to share his knowledge on some of the intricacies of microwave amplifier design.

His talk addresses the topic of lossless feedback networks for three types of amplifiers:

1) High Gain - Mason's Unilateral Gain Amplifier achieved by designing a lossless feedback network to cancel (unilateralize)  $S_{12}$ , the reverse gain of the amplifier, thus not having to compromise gain for stability. Several feedback topologies are examined.

2) LNA - Vendelin 1975 Low noise design using emitter/source inductors to achieve  $F_{min}$  and  $S_{11}' = 0$ . This examines how to optimize the input match of an amplifier while simultaneously obtaining low noise figure.

3) HPA - The dual of 2) where max P1dBC is achieved with  $S_{22}' = 0$ . This examines a high power amplifier optimized for output match,  $S_{22}'$  at the 1 dB compression point.

Some of this talk was published in IEEE Microwave Wireless Components Letters, March 2003, p 110.

George Vendelin becomes an IEEE Life Fellow this month. He currently teaches at Stanford, Santa Clara University, San Jose State University, and University of California Berkeley Extension since 1976. His research interests includes nonlinear models of microwave devices and circuits and is one of the authors of 'Microwave Circuit Design - Using Linear and Nonlinear Techniques'; 2nd edition late 2003. He also wrote 'Design of Amplifiers and Oscillators by the S-Parameter Method'; 1982, John Wiley. He is a consultant for microwave circuit designs.

# ISQED 2003 Report

The 4th International Symposium on Quality Electronic Design, ISQED 2003, was successfully held on March 24 - March 26, in DoubleTree hotel, San Jose, CA. Repeating the past ISQED events, the Organizing and Technical committees as well as all the technical contributors and speakers made tremendous efforts to make this a premier conference and a valuable event, worthy of participation.

This year's conference coincided with the worldwide economic down turn, US lead war into Iraq, and travel concerns over SARS. The impact of this was certainly felt in the attendance; particularly our European and Asian attendees had to cancel their previously planned travel to the conference. As an aside, many other conferences were cancelled. Nevertheless we were fortunate to have a reasonably strong attendance and an enthusiastic audience. The diversity of the participants, insofar as it applies to the various that were represented, validates our vision for the conference as the ideal venue where the multitude of disciplines in the electronics industry can interact, share and collaborate to solve common problems. Additional validation comes from the stature of six plenary speakers who shared with the audience their view of the industry and their vision for the future. Supplementing the plenary talks were 3 panel discussions, which addressed some very critical issues facing the industry and generated some very lively discussions as well as providing unique viewpoints. Since the ISQED mission is to promote the communication and close cooperation between all the disciplines involved with the electronic design it was very encouraging that this year's audiences, similar to the last year, came from not only the design community but also included strong participation from EDA, software, Semiconductor, and other disciplines. As usual, the quality of keynote speeches, panels, tutorials and technical sessions were outstanding throughout the event.

ISQED 2003 was held in technical sponsorship of IEEE EDS, IEEE CPMT, and in cooperation with ACM/sigDA which created the CD version of the proceedings. IEEE Computer Society produced the print version. ISQED'03 corporate and Media sponsors were: Synopsys, Magma Design Automation, Numerical Technologies, Ammocore, Ascend Design Automation, RubiCAD, Nassda, Penwell/Advanced Packaging, IBSystems/EDAtoolsCafe, and EE Times.

## Plenary Sessions

One of the key features of ISQED 2003, coined as the "Hall Mark" of the conference by participants, was the plenary sessions featuring excellent keynote speech by several world-renowned leaders, from the industry and academia. A total of six keynote speeches were delivered in two plenary sessions, organized by the plenary chairs Kris Verma and Lech Jozwiak, who have been involved with ISQED since the first event in 2000.

The format of the plenary sessions was conceived by the ISQED founder, Ali Iranmanesh, to convey the strong multidisciplinary aspect of the conference. The Tuesday session was chaired by, Bharath Rajagopalan, the organizing committee chair, and Kenneth Shepard, the technical programs chair. Chi-Foon Chan, president and COO of Synopsys, and the chair of the ISQED steering committee, moderated the plenary session on Tuesday morning. All past presentations are available on the conference web page at [www.isqed.org](http://www.isqed.org).

## Following topics were covered:

Platform Leadership in Ambient Intelligence Era- Bob Payne-CTO, Phillips Semiconductor. The main message was to have Platform approach to create new designs in shortest possible time.

Quality of SoC Design and Implementation for real Manufacturability- Susumu Kohyama-Sr. VP, Toshiba Corporation. Dr. Kohyama emphasized the "quality culture" in design phase of SoC for real manufacturing of complex multi-million gates device.

Quality Challenges of the Nanometer Design Realm-Aurangzeb Khan- VP/ GM-Cadence Design System. Mr. Khan addresses the importance of the EDA tools and Methodology to achieve the desired results in this complex SOC era.

IC Designer's Need in deep Sub-micron Era-Rajeev Madhavan-CEO- Magma Corporation. Mr. Madhvan gave very energetic presentation relating the role of Software and hardware in complex SoCs.

Closing the gap between ASIC and Custom Design-Michael Reinhardt- CEO-Rubicad Corporation. Mr. Reinhardt presented a very realistic picture of 300 mm Fab capacity utilization in coming years with full of information and data on 200 mm existing silicon fabs. He gave a good perspective for custom design performance v/s traditional ASICs approach.

A VLSI System Perspective for Microprocessors Beyond 90 nm- Shekhar Borkar -Intel Fellow- Intel Corporation. Mr. Borkar emphasized the need of "Power aware Electronics" to have full utilization of shrink path of CMOS technology.

## Panel Discussions

At ISQED 2003 the highlights at the evening were two interesting panel discussions with high profile executives from a variety of different companies. All panels included members from the academia, design service, AISC, Semiconductor and EDA companies as well as from wafer fabs.

Monday evening's panel was devoted to the million-dollar question: "Is Quality a Design Constraint for Sub 100nm designs?"

The panelists presented and discussed the design challenges, which

*Continued on page 14*

# OEB Industry Applications

## THURSDAY OCTOBER 16

### THURSDAY OCTOBER 16

OEB Industry Applications Society

Subject: **Medium Voltage Arcing Faults and Arc Resistant Switchgear**

Speaker: Jim Bowen (Powell Electrical Manufacturing Co.)

Time: No-host social at 5:30 p.m., presentation at 6:15, dinner at 7:15, presentation continues at 8:00

Place: Marie Callendar Restaurant, The Garden Room, 2090 Diamond Blvd., Concord (nearby to Concord Hilton Hotel) 925 827-4930 for directions

Cost: (dinner) \$22 for IEEE members, \$25 for non-members.

RSVP: (by 10/15) Gregg Boltz, 925 210-2571 or <mailto:gboltz@brwncald.com>

## Medium Voltage Arcing Faults and Arc Resistant Switchgear

The October 16 meeting of the IEEE Industry Applications Society for the Oakland East Bay Section will feature a talk that will focus on medium voltage arcing faults and how an arcing fault behaves in a switchgear environment. The nature of the arcing fault is different from bolted faults and medium voltage arcing faults are very different when compared to low voltage arcing faults.

Switchgear designed and tested to protect personnel for the arcing fault is becoming more and more common place. This presentation will cover the standards which arc resistant equipment are tested to, and the acceptance criteria that apply. Safety enhancement features typically found in the arc resistant switchgear will also be reviewed. In addition, the discussion includes videos of fault in a test lab environment and an understanding of what is involved in the testing. This talk will be an informative update for all electrical professionals.

The speaker will be Jim Bowen from the Powell Electrical Manufacturing Co. Jim has been with Powell for five years and holds the post of technical director. He provides technical leadership, training, and mentoring in the utilization of equipment rated 38 kV and below. He also authors the Powell Technical Briefs, a popular series of articles (1 to 3 pages in length) that address technical problems commonly found in the electrical power workplace. The company is based in Houston, Texas and is a major supplier of electrical power distribution equipment.

Prior to joining Powell, Jim worked at Exxon for 18 years in a variety of positions in engineering, maintenance, and start-up. He also held the post of regional engineer for Exxon Chemicals Europe for three years. Jim has worked in all facets of electrical engineering involved with the petrochemical process, and was assigned to large projects, which included co-generation, high voltage gas insulated switchgear, and large variable speed drives. Prior to Exxon, he spent three years with SIP Engineering. Jim received his BSEE degree from Texas A&M University and he holds a PE license in Texas. He is the author of a number of papers presented at the IEEE PCIC conference and has taught at the PCIC Electrical Safety Workshop.

**SATURDAY OCTOBER 18**

SF Power Engineering Society

Subject: **Distributed Generation  
Fundamentals Workshop**

Speaker: Various

Time: 8:00 a.m. to 4:00 p.m.

Place: San Francisco State University

Fee: See SF PES website

RSVP: Mr. Shimo Wang at (650) 450-1306 or  
shimo\_wang@ieee.org

Web: [http://www.ewh.ieee.org/r6/san\\_francisco/  
PES\\_PEN/DGFlyer.htm](http://www.ewh.ieee.org/r6/san_francisco/PES_PEN/DGFlyer.htm)

**Distributed  
Generation  
Fundamentals  
Workshop**

Distributed Generation (DG) is an important local resource that may enhance the electric service reliability and the power quality at a local facility. California is promoting clean renewable distributed generation as a key component of its energy system. Clean distributed generation can enhance the state's environmental goals.

This commitment to efficient, clean, and renewable energy resources provides vision and leadership to others seeking to enhance environmental quality and moderate energy sector impacts on climate change. What are DG principles? What are DG characteristics? What are the distribution system characteristics? How will DG impact power system operations? What are the DG standards and references? Please join our one-day workshop to find out the answers.

Topics to be covered in the course include: DG Principles; Distribution System Characteristics; Typical DG Systems & DG Applications; System Impact Review; and Interconnection Study DG Standards and References.

Instructors: Dr. ShySheng Liou - San Francisco State University; Robert Wichert - US Fuel Cell Council; Willie Chew - Pacific Gas and Electric Company; Dr. Mohammad Vaziri - Pacific Gas and Electric Company; Gary Olson - Cummins; and Chuck Whitaker - Endecon.

designers face if they design for deep sub micron (below 100nm). These include very high masking costs, new interconnect materials and parasitic phenomenon, significant re-engineering at the device level due to changes in basic device performance, very high gate count and pin count designs, complexity in high pin count packaging & test, and finally reduced product life in the marketplace do to the rapid rollout of new technologies. One of the trade offs that is taking place in the industry to address these issues is the decision toward “design existence”, which is the selection of the “first functional implementation” of a design, over “design quality” which is the selection of the “optimal implementation” of a design.

The panelists discussed the trends with respect to the re-targeting of the design quality issues from the SOC level to the flow and device levels and the impact on this “shift” on the manufacturability of the resulting designs. They addressed the use of pre-tested IP as a quality metric, the coverage and quality of the EDA design and validation tools, the correlation of these metrics to the actual manufacturing process and the impact of post fabrication process steps (packaging, test, etc) on the yield of the resulting design.

The panel was organized by Pallab Chatterjee, SiliconMap, CA.

At Tuesday evening the panel topic was “IC & Package Co-Design: Challenge or Dream?”

In recent years, major breakthroughs have occurred in packaging technology, which have led to the industrialization of several kinds of new packages, more powerful, and yet more flexible, in the attempt to cope with the challenges posed by multi-million gates and multi-GHz systems-on-a-chip (SOC). While offering a great deal of opportunities, ball-grid array (BGA) substrates, flip-chip and multi-stacked dies require an unprecedented level of integration between IC and package design and verification.

The panelists discussed that this integration requires a change in methodology, with the availability of new EDA tools, and a major shift in the profile of the designers and engineers involved which, to a certain extent, have to acquire each other competences.

It turned out that although necessary, this couldn't be given for granted. While BGA is a reality, flip-chip is still a question mark for the majority of the applications, due to both cost reasons and lack of commercial EDA tools. Marco Casale-Rossi of ST Microelectronics, Italy, organized this panel

On Wednesday afternoon a third panel picked up the quality issues in EDA tools: “Hidden Quality, Crouching Customer - How much does the Quality of EDA Tools Impact Electronic Design?”

This panel examined the core issues of quality in EDA products and the impact on electronic design — from the viewpoints of customers, EDA vendors and independent analysts.

Nowadays design engineers face incredible challenges keeping up with increasingly complex technology and time-to-market pressures. Many design engineers facing these challenges say that quality problems with their EDA tools cost them dearly in lost productivity and in missed deadlines. At the same time, the same design engineers also say that they urgently need better technology, features, and special functions in

the EDA tools they use in their work.

Panelists discussed questions like: How much quality is enough to keep the industry moving at its fast pace? Is quality a hidden dragon that could cause customers to crouch in fear? What are the costs and who will pay for higher quality? Can EDA customers have their cake and eat it too? The panel was organized by Giora Ben-Yaacov of Synopsys

### **Technical Papers and Awards**

A great collection of papers covering many disciplines were presented in a total of sixteen sessions. The technical committee members selected these papers for presentation from many excellent submissions. The technical program for ISQED 2003 was assembled by the technical program committee, which includes international experts from industry and academia. This year, a total of 39 papers were accepted for regular presentation from 119 papers submitted to ISQED 2003. Because of the high quality of this year's submissions, an additional 16 short papers were accepted. The technical program also includes several invited papers from leading experts in the field. The ISQED 2003 best paper award granted to Takashi Sato of Hitachi, and Hiroo Masuda of Semiconductor Technology Academic Research Center, Japan for their paper titled “Design and Measurement of an Inductance-Oscillator for Analyzing Inductance Impact on On-Chip Interconnect Display”.

### **Tutorials**

The conference commenced with the popular tutorial sessions, organized by Tuna Tarim and Enrico Malavasi, on Monday, March 24. There were a total four parallel tracks, featuring experts from around the world. The tutorial sessions covered a variety of exciting and timely topics such as Test Methodologies for Quality Design, Testing and Yield of Integrated Circuits, IC and Package Co-design, and Design for Reliability. Topics to be presented includes: Testing and Yield of integrated circuits, Test structures for circuit yield assessment and modeling; Design based yield improvements (DBYI); Yield in flash memory - methodology, modeling and design issues; Enhancing the Silicon-Package Interface Through Their Concurrent Design and Verification; A package design perspective - “It will be BGA and flip-chip”; An IC design perspective - “Why would we choose flip chip?”; Noise analysis for 0.13um and beyond; NBTI/HCI Modeling and Full-Chip Analysis in Design Environment; overview and circuit design considerations.

### **Conclusion**

In summary, the ISQED organizing committee is very gratified that the vision for this conference as a unique venue where the various stakeholders from the industry can meet to solve common problems is the vision that is unfolding. We anticipate continued evolution of this conference moving toward its 5<sup>th</sup> year. The next ISQED 2004 is planned for March 22 - 24, of 2004 in San Jose, CA. All inquiries about the conference should be addressed to [isqed@isqed.org](mailto:isqed@isqed.org). Further information about the conference is available in the conference web site at <http://www.isqed.org>.

**TUESDAY OCTOBER 21**

SCV Magnetics Society

Subject: **Beyond Disk Drives: Probe Storage**

Speaker: Jim Brug (Hewlett-Packard  
Laboratories)

Time: Coffee and conversation at 7:30 p.m.,  
presentation at 8:00

Place: Komag, 1710 Automation Parkway,  
San Jose

RSVP: Not required

**Beyond disk Drives —  
Probe Storage**

Disk drives are the workhorses of the computer industry, storing vast amounts of information on the network or on our desk. Yet they are far from perfect. Some of the concerns about disk drives are the amount of power being consumed; not every application requires the huge storage capacities being achieved; and PC's aren't realizing their full performance potential with the slow access times.

The coming of age of MEMS technology is now allowing small micromachined motors to replace spinning disks in a new type of low cost, high capacity storage device. Jim Brug will describe the ongoing research at Hewlett-Packard Laboratories in probe storage at the October 21 meeting of the Santa Clara Valley Magnetics society.

Jim Brug manages the Advanced Storage Department at Hewlett-Packard Laboratories in Palo Alto. His group is developing storage and memory technologies using new materials and fabrication methods. He received his PhD from Yale University in applied physics in 1984 and he has since been at HP Labs doing research on magnetic recording heads, magneto-optic media, magnetic memory and scanned-probe storage. He has been a visiting scientist at the National Institute for Standards and Technology and he managed the National Storage Industry Consortium's project on Ultra-High Density Recording Heads.

**TUESDAY OCTOBER 28**

SCV Lasers &amp; Electro Optics Society

Subject: **Electronic perception technology:****Everyday Devices that See**

Speaker: Dr. Cyrus Bamji (Canesta)

Time: Pizza social at 7:00 p.m., presentation at 8:00

Place: National Semiconductor Credit Union Large Auditorium, 955 Kifer Road, Sunnyvale

RSVP: [rsvp@silicavalley.com](mailto:rsvp@silicavalley.com) to indicate how many attending pizza social

## Electronic Perception Technology: Everyday Devices that See



Electronic perception technology is a new, low-cost, single-chip imaging technology that creates 3D images of its nearby surroundings in real time, enabling everyday devices to “see.” Unlike the sensors in digital still and video cameras that see the world as flat images, Canesta technology can additionally compute the distance from the sensor of every single pixel in the image, in real time.

The first application of this technology is a chipset that can be integrated into mobile devices to provide a projection keyboard. Users simply put the device on any table and an image of a keyboard is projected onto the table in front of them. The user simply types on the table to enter text into the device. This innovation is expected to support more advanced applications (such as wireless email) in convenient form-factor devices such as cell phones and PDAs.

When everyday devices can perceive the world around them, entirely new levels of functionality and convenience become possible. A PDA that can watch its user’s fingers type is just the first example. Other applications in a variety of markets could include doorknobs that recognize members of the household and open automatically, automobiles that can sense their occupants to deploy airbags appropriately, and security systems that can more easily tell the difference between an illicit action and an authorized activity. When this capability can be added to virtually any product in a cost-efficient manner, designers will let their imaginations run free.

Dr. Cyrus Bamji will demonstrate this technology at the October 28 meeting of the Santa Clara Valley Lasers & Electro Optics Society. Dr. Bamji is a founder and CTO of Canesta. He has nine years of experience working in Electronic Design Automation. Previously he held the position of an architect, a director level position, at Cadence. He has an SB in math, SB in CS, SM and PhD in EECS from MIT.

He has interest in and is conversant with a wide variety of technical disciplines including physics, math, electrical engineering, and computer science. His work in the area of hierarchical layout compaction has produced a quantum improvement in the state of the art in this area and is recognized as a landmark achievement. He is the author of over 15 conference papers and journal articles presented at top rated IEEE Conferences. Of these papers, three have won the best paper award at their respective conferences. He has been granted seven patents, with more being filed. He is also the author of a book on Compaction Leaf Cell and Hierarchical Compaction Techniques. He is fluent in English and French and can get by in four other languages.



Jim V. Leonard, PE  
*2003 IEEE-USA President*

## Engineer Mentors Sought for Future City Competition

Across America, thousands of engineers volunteer annually to serve as mentors for students in the National Engineers Week Future City Competition. As National Engineers Week 2004 co-chairs, IEEE/IEEE-USA and Fluor Corporation invite engineers from every discipline to become volunteer mentors and help students get a better view of engineering.

Interestingly, the engineers who guide the students from conception to design to construction of their future cities consistently say that one of their finest rewards is how the students give them a better perspective of their own lives.

"It's helped me not be so narrowly focused," said Tony Arikol, P.E., an engineering consultant in Baton Rouge, La. "Sometimes you get tunnel vision. Young people are a lot more creative as thinkers. They help you look outside for novel solutions. And when you look for novel solutions, you find them."

"It makes me feel young again," said Jean Eason, an electrical engineer and regional coordinator for the Dallas/Fort Worth area Future City Competition. "It's invigorating. I'm struck by how concerned the kids are for the environment and for the future of the planet."

In the competition, teams of three seventh- and eighth-graders design and build model cities of tomorrow. The students, with the help of a teacher and engineer-mentor, must design a city that functions, write an essay and abstract, and defend their city before a panel of judges.

Students begin their cities at the start of the school year, working during and after school and through holiday breaks. Regional competitions are held in January. First-place teams (including the engineer mentor) win all-expense-paid trips to Washington, D.C., for the national finals during National Engineers Week, 22-28 February, 2004.

For more information, contact Carol Rieg, Future City Competition national director, at 877-636-9578, or via e-mail at [CRieg@futurecity.org](mailto:CRieg@futurecity.org). Visit [www.futurecity.org](http://www.futurecity.org) for a list of participating regions and regional coordinators.

Subject: **The Top Ten Ways Women in the Workplace Shoot Themselves in the Foot**

Speaker: Nora M. Denzel (Hewlett-Packard)

Time: Social and refreshments at 6:45 p.m., presentation at 7:00

Place: The Dragon's Den of Cogswell Polytechnical College, 1175 Bordeaux Drive, Sunnyvale

RSVP: [wendycwong@ieee.org](mailto:wendycwong@ieee.org)

## The Top Ten Ways Women in the Workplace Shoot Themselves in the Foot



Nora Denzel, HP, will be the featured speaker at the October 29 meeting of the Santa Clara Valley Women in Engineering Society. This exciting talk will acquaint you with the ten most common mistakes women make in trying to climb the corporate career ladder.

You will learn first hand what the mistakes are and how to combat them from someone who has been there. Using a lot of humor and personal experience, Nora will share with you what she learned as she climbed the corporate ladder at IBM to become one of their youngest executives by the age of 33! She will talk candidly on how she did it, and how you can do it at an even faster pace.

After this session, you will not only be able to *recognize* what the most common mistakes are, but you will have heard practical experience on how to *avoid* them.

Nora M. Denzel is senior vice president and general manager of HP's Software Global Business Unit. She has worldwide responsibility for the entire HP software portfolio, including the industry leading OpenView and OpenCall management software product lines.

Ms. Denzel joined HP in 2000 as the vice president of the storage business and was promoted to her current position in May 2002. Prior to joining HP, she was senior vice president and a corporate officer of Legato Systems, Inc. where she was tasked with running the engineering and technical support operations of the company as it grew from \$50M to over \$250M in revenue. She began her career at IBM in San Jose as an engineer and left IBM in 1997 after serving in several engineering, marketing, and executive posts in the storage division.

She was recognized by the YWCA of Santa Clara County with a Tribute to Women in Industry award for her contributions to the substantial revenue growth of IBM's storage software and was named in the top 20 movers and shakers in the worldwide storage business by *Storage Magazine*.

She holds a BS degree in computer science from the State University of New York and an MBA from Santa Clara University. She serves on the boards of Women in Technology International and on the advisory board of the Business School at Santa Clara University.



# *11<sup>th</sup>*

## *Annual*

### *Electrical Safety*

#### *Workshop*

*February 10-13*

*Oakland, California*

The IEEE Industry Applications Society Electrical Safety Workshop is requesting proposals for presentations at the 11th Annual Electrical Safety Workshop to be held February 10-13, 2004 in Oakland California. Preference will be given to proposals aligned with the theme for the 2004 Workshop: Electrical Safety during construction, commissioning, operation, and maintenance of the Electrical System! Non-commercial presentations are requested that advance the Mission of the Electrical Safety Workshop to:

- Accelerate the application of breakthrough improvements in human factors, technology, and managing systems that reduce risk of electrical injuries,
- Stimulate innovation in overcoming barriers,
- Change and advance the electrical safety culture to enable sustainable improvements in prevention of electrical accidents and injuries.

#### **Submission Calendar drop dead dates:**

- June 15, 2003 : Submittal of 200 word abstract to Technical Program Chair
- August 1, 2003: Notification of acceptance of submitted proposal
- December 15, 2003: Submittal of finished presentation materials

#### **Submit proposals and abstracts to:**

Jim Bowen  
Technical Program Chair  
2003 IEEE IAS Electrical Safety Workshop  
Powell Electrical Mfg.  
Tel: 713-948-4511  
Email: [JBowen@Powl.com](mailto:JBowen@Powl.com)

**Please check our website for updates and latest information at:**

[www.ieee-pcic.org/safety/esw.htm](http://www.ieee-pcic.org/safety/esw.htm)



**WEDNESDAY OCTOBER 29**

SCV Reliability and Power Electronics Societies

Subject: **Power Supply Reliability – an Oxymoron?**

Speaker: Dave Christiansen (HP) and Brooks Leman (Fyre Storm)

Time: Refreshments at 6:30 p.m., presentation at 7:00

Place: HP-Cupertino Oak Room, Bldg 48. (corner of Pruneridge Ave. and Wolfe Rd.)

RSVP: Not required

Web: <http://www.ewh.ieee.org/r6/scv/rs/index.html> for more information and a map

## Power Supply Reliability - An Oxymoron?

There are many pitfalls in obtaining a power supply with good reliability. Dave Christiansen and Brooks Leman will discuss the important elements in power supply reliability and some ways to avoid the pitfalls at the October 29 joint meeting of the SCV Reliability and Power Electronics Societies.

Topics covered in this presentation include: Is there such a thing as a million hour MTBF power supply?; How do you pick a good supplier and what do you do once you have one?; MTBF calculations and specification; Stress analysis; Evaluating transient conditions, e.g., power on-off cycles; and Testing, including power supply dynamics and redundancy (if it exists).

David Christiansen is a member of the Reliability Engineering Department for Hewlett-Packard's NonStop Enterprise Division. He comes with 40 years experience in the computer industry, and has been with the HP reliability department since 1989. He has been instrumental in developing prediction methods, data retrieval and reporting techniques, and corrective action processes. He received his BSEE and MSEE from the University of Wisconsin, and MSQA from San Jose State University. He is a Life Member of IEEE.

Brooks Leman is a power supply engineer at Fyre Storm. He has worked in a variety of power management and engineering positions at Rolm, Power Integrations, and Hewlett-Packard's NonStop Enterprise Division. He has over 20 years experience in power electronics in the military, server, and consumer electronics industries and has taught a graduate power electronics course. He has a BSEE and MSEE from Santa Clara. He is the vice chair of the SCV Chapter, IEEE Power Electronics Society.

**WEDNESDAY OCTOBER 29**

SCV Engineering Management Society

Forum Subject: **Creating Successful Mentoring Relationships to Accelerate Learning**

Speaker: Kathie Sinor (Career Development Consultant) and Helen Gracon (Consultant)

After-dinner Subject: **Planning and Executing Fast-Track Projects**

Speaker: Dr. Raymond Levitt (Stanford University)

Time: Forum at 6:00 p.m., dinner at 7:00, presentation at 7:45

Place: Wyndham Garden Hotel, 1300 Chesapeake Terrace, Sunnyvale (off Lawrence Expressway at Hwy 237)

RSVP: <http://www.ieee-scv-ems.org> (Info: Rich Hendrickson, 408 203-3462.

Cost: (with reservations 10/24) \$20 (IEEE member), \$25 (non member), \$5 surcharge thereafter. (cash or check at the door). Student IEEE members, \$5

## Tools for Accelerated Learning and for Fast Track Project Management

On October 29 the Santa Clara Valley Engineering Management Society's dual-presentation dinner meeting includes a before-dinner forum on organizational learning through mentoring. Following networking and a sit-down dinner, the after-dinner topic will review a variety of methodologies and tools to confidently manage the most aggressive project schedules and staffing for execution of fast-track initiatives.

Forum presentation

### **Creating Successful Mentoring Relationships to Accelerate Learning**

Ask successful people how they got to where they are now, and most will give credit to a mentor who accelerated their learning along the way. Mentoring can be formal or informal, successful, a disaster, or somewhere in between.

At this EMS forum, learn how to set up the mentor relationship for success, and the role and responsibility of both parties in the relationship. In more formal mentor and mentee arrangements, the developmental plan of the mentee plays a significant part in the design of the program. Negotiated agreements frame the relationship in order to ensure that both parties get what they need. From an organizational and personal viewpoint, there is a return on your investment, which can be demonstrated. Learn how to set up a program pilot in your organization and the basic elements that will ensure success.

Co-presenter Kathie Sinor has been a mentor and a mentee over most of her 20 year career in Human Resources, and in business. Recently, as a manager at Sun University, Sun Microsystems, responsible for the management, teams and new hire curriculum, she experienced how getting the right mentor at the right time saved her career from derailing.

Kathie mirrors the values and best practices learned from training managers, as well as being a manager in her own company of 200 employees, and in the high tech world. She has worked at all levels in an organization from CEO to mid-level manager to professional staff. Kathie earned her BA from UCLA and Masters from University of San Francisco in human resources and organizational development.

*Continued on next page*

During the time she was completing her masters degree, she was working at National Semiconductor and was fortunate to work with organizational gurus, such as David Sibbet and Peter Senge, to learn, then teach, the importance of visioning and teamwork built on collaboration and commitment. She is now an independent consultant serving numerous clients.

In Helen Gracon's 20 years experience in career counseling, she has worked with both employed and unemployed Silicon Valley professionals in fields ranging from high tech to manufacturing. She has designed and implemented both retention and downsizing programs. Her recent experience has been developing, implementing and advocating global mentoring that accelerates learning in high tech companies, speaking to audiences at IEEE, ASQC, Amdahl, Apple, Raychem, Lockheed, UC Berkeley Business Alumni, Women in Aerospace, and others.

Helen co-authored an article called, "Lay-Off Should Come Last" for *IEEE Spectrum magazine*. She has been a consultant for Raychem, Apple, and Sun Microsystems, and a program director for ProMatch, a nationally recognized career development center. Helen is a Nationally Certified

Career Counselor and holds a Masters Degree in counseling.

After-Dinner presentation

### **Planning and Executing Fast-Track Projects**

The competitive need to innovate while decreasing time-to-market requires many firms to schedule multiple product-development projects aggressively and then execute them concurrently. The resulting exponential increases in coordination and rework for interdependent project tasks challenge the organization's ability to rely on intuition or existing project scheduling approaches, and taxes tool capability to plan and execute fast-track projects.

In his presentation, Prof. Raymond Levitt will review a variety of methodologies and tools — including PERT Simulation, Critical Chain, and SimVision - that allow managers to determine the most aggressive project schedules and staffing levels that they can confidently use to execute their fast-track initiatives successfully. This program will feature a drawing for a free online Stanford Advanced Project Management course. To learn more about the program, connect to: <http://apm.stanford.edu>. Stanford has a program that goes

beyond the project management body of knowledge concepts and specialized project management training

Dr. Levitt is professor of civil and environmental engineering, academic director of the Advanced Project Management Executive Education Program, and director of the Collaboratory for Research on Global Projects, at Stanford University. He has worked with global companies in the design of project/matrix organization structures, work processes, and IT applications to support project work.

His current work focuses on modeling and simulating the significant institutional costs that can arise in global projects. Levitt's Virtual Design Team research group has developed new micro-organization theory and computer simulation tools to design organization structures for fast-track product development. He has consulted to numerous Fortune 100 companies on organization design for project execution. Dr. Levitt co-founded, and is a director of, Design Power, Inc., Vité Corporation, and Visual Network Design, Inc.

## **LONG TERM DISABILITY CLAIMS**

Since 1977 our firm has been representing and assisting professionals in pursuing LTD claims, under both individual insurance policies and ERISA regulated group policies.

**Call us for a free consultation.  
Our practice is limited to LTD claims only.**

### **LAW OFFICE OF SILVER & TAUBE**

300 South First Street, Suite 205  
San Jose, California 95113  
(408) 298-9755 • fax: (408) 298-9699  
[www.SilverandTaube.com](http://www.SilverandTaube.com)

UNUM • MET LIFE • AETNA • CIGNA • PAULREVERE • CNA • PROVIDENT • KEMPER •  
STANDARD • SUN LIFE • CANADA LIFE • RELIANCE • MUTUAL • PRUDENTIAL •  
OTHERS

**FRIDAY NOVEMBER 7**

SCV Power Engineering & Industry  
Applications plus SF Industry Applications  
Societies

Subject: **IEEE Short course: Successful  
Design, Implementation & Testing of  
Electrical Grounding Systems for  
Facilities**

Instructor: Roy "Chip" Whitten (senior  
applications engineer of Lyncole  
Industries)

Time: 8:00 a.m. to 5:00 p.m.

Place: Square D Co., Suite 200, 6160  
Stoneridge Mall Rd., Pleasanton

Fees: \$140.00 IEEE members, \$160.00  
non-members

Contact: James Alvers, 925-730-3105,  
alversj@squared.com or  
Finn Schenck, 925-730-3148,  
schenck@squared.com

**IEEE Short Course:  
Successful Design,  
Implementation & Testing  
of Electrical Grounding  
Systems for Facilities**

Proper grounding is of course essential for safety in electrical systems of industrial and commercial facilities. In addition, well-grounded systems are required to insure power-quality and reliability as well.

So, are you spending thousands of dollars to repair damage to your sensitive electronic equipment due to lightning strikes or power surges? Is your facility plagued by mysterious electrical problems? Are you designing new facilities?

The solutions all start with proper grounding. Please join us for a short course that addresses how to successfully design implement and test and electrical grounding system. Here's what you'll learn:

- Purpose/Definition of Grounding; Grounding Design Theory; Factors that Influence Results; Soil Characteristics; Soil Resistivity; and Effects of Moisture & Temperature.
- Characteristics of Ground Electrodes; Spheres of Influence; Rod Length vs. Resistance; and Number of Rods vs. Resistance Design Processes.
- Types of Grounding Electrodes; Water Pipes/Driven Rods & Grids; Ground Plates; Chemical Wells/UFER; and XIT™ Systems.

- Design Processes; Site and Soil Survey; Design Calculations; Installation; and Final Inspection and Resistance Testing.

- Ground Resistance Testing; Fall-of-Potential Test; Clamp-On Resistance Testers; and Ground Resistance Monitor GRM 2000RS.

- Bonding; Coaxial Grounding Kits; Mechanical Connections; Exothermic Welding; and High Compression Crimps.

- Communications Applications; Exterior Grounding; Integrated/Isolated Grounds; and Raised Floor Grounding. Lighting Protection; Basic Theory of Protection; and NFPA Art. 780.

- National Electrical Code; Art. 250.

- Surge Protection Devices; Types of surges; and Methods of Protection.



*IEEE Consultants' Network of Silicon Valley*



**Do you have to get more  
Technical Projects  
completed with fewer  
resources while  
still compressing  
budgets and time?**

**Our Consultants' can help get your projects moving ahead quickly**

Is your team not producing results, or do you need qualified technical help fast? If so, our consultants can get you moving ahead quickly. When your existing staff is overwhelmed, stuck in outmoded development methodologies, or lacking in modern expertise, we have experts you can use and reduce overall costs, too.

**Skill and Experience**

Our technical and project management professionals are experienced and skilled independent contractors that are ready to come up to speed quickly on your projects. Unlike other Consultants, our

members are not "just between jobs". We have years of experience in helping companies like yours reach their technical project goals.

**Visit: [www.ieee-sv-consult.org](http://www.ieee-sv-consult.org)**

Check out our website to see what we can offer your project. Our consultants' capabilities are right there, and we are ready to help you immediately.

On the website is a referral service and the on-line brochures of our members. If you wish to speak with someone about our services or consultants, call or email any of our Officers, and we will be happy to assist you.

**We have been providing excellent service to satisfied managers for years!**



*IEEE Consultants' Network of Silicon Valley*

### Patent Agent

Jay Chesavage, PE  
MSEE Stanford  
3833 Middlefield Road, Palo Alto, CA 94303  
**patents(at)chesavage(dot)com**  
TEL: 650-494-9162  
FAX: 650-494-3835

### Patent Applications Continuity Backup

Hans, PE, MSEE Stanford  
USPTO reg. 35,397, VP-IP,  
*patents@jdsconsulting.com*  
Palo Alto, 650-494-1458

### DR. FLOYD M. GARDNER

Consulting Electronics Engineer  
*Phaselock, Communications  
Synchronization, Signal Processing*  
**1755 University Avenue  
Palo Alto, CA 94301 (650) 328-8855**  
Website: [www.fmgardner.com](http://www.fmgardner.com)

Wi-Fi, UWB, WBA, 3G, Bluetooth, Telematics,  
Satellites, DoD ...

#### Wireless Systems

**Contract R&D, Technical consulting  
Antenna Design & Development, RF/  
Subsystem, Radio Frontend Integration, Test,  
Reference Designs from Concept to Products**  
Contact Dr. Jamal S. Izadian @  
**ANTENNE COMMUNICATION, LLC, (408)927-6880**  
[info@antennem.com](mailto:info@antennem.com), [www.antennem.com](http://www.antennem.com)

### James Long, Ph.D., P.E. Analog and RF Consulting Engineer

- new designs
- design reviews
- troubleshooting existing designs

(408) 733-8329 [www.Analog-RF.com](http://www.Analog-RF.com)

### Mixed-Signal IC Development

- From Inception to Production Transfer
- Turnkey, Design Services & Consulting
- Design Reviews & Trouble Shooting

#### Mixel, Inc.

*Excellence in Mixed Signal Design*

**(408) 274-2736**

[sales@mixel.com](mailto:sales@mixel.com) [www.mixel.com](http://www.mixel.com)

### SHAX Engineering and Systems

#### Electronics Design Services

- Analog and Digital circuit design
- VHDL/Verilog coding and synthesis
- ASIC/FPGA from concept to production

**(650) 966-1835**

[ishakour@shax-eng.com](mailto:ishakour@shax-eng.com) [www.shax-eng.com](http://www.shax-eng.com)

### Digital Signal Processing for Telecommunications

#### Stevan Bradley

Programming and consulting services

[www.illico.com/illico/bradley.htm](http://www.illico.com/illico/bradley.htm)  
555 Hamilton Ave #120, Palo Alto, CA  
(650) 327-7651

TECHNOLOGY WRITER  
TECHNICAL COMPOSITION, INC.

#### R. C. AYERAS

*WRITE, FORMAT, ILLUSTRATE, HARDCOPY, ONLINE,  
SOFTWARE, HARDWARE, SYSTEMS, COMPONENTS*

Tel: (408) 262 7606 Fax: (408) 262 5941  
[r.c.ayeras@technology-writer.com](mailto:r.c.ayeras@technology-writer.com)  
[www.technology-writer.com](http://www.technology-writer.com)