CHAPTER MEETINGS

SCV-CE - 1/30 | Consumer Electronics Show Download - presentations on observations from the show in Las Vegas ... [more]
SCV-Rel - 1/31 | Best of ISTFA - highlights from the Int'l Symposium for Testing and Failure Analysis, in Austin ... [more]
SCV-LEOS - 2/6 | Large Scale Photonic Integrated Circuits for Optical Fiber Transmission - ... [more]
SCV-CPMT - 2/7 | Recipe for a New Embedded Component: Connectors - using photolithography for better dimensional scalability, electrical performance ... [more]
SCV-MTT - 2/8 | Impedance Matching Networks and Fundamental Limits - two surprising strategies to achieve results ... [more]
SCV-SPS - 2/12 | A/D and D/A Converters with Integrated High-speed Compression - Samplify's lossless/lossy modes ... [more]
SCV-EDS - 2/13 | Recent Progress in Photovoltaics - An IMEC View - European solar cell roadmap, crystalline silicon, organic cells ... [more]
SCV-EMC - 2/13 | Taking the Guesswork out of EMC Design using Numerical Simulations - cost-effective comparisons ... [more]
SCV-CNSV - 2/15 | Ten Tips for Leveraging Blogs and Wikis in Your Consulting Practice - social software technologies ... [more]
OEB-IAS - 2/15 | Short-Circuit Current Rating of Industrial Control Panels - definitions, codes, examples ... [more]
SCV-SSC - 2/15 | RF ESD Protection Strategies -Design and Performance Trade-off Challenges - CMOS and BiCMOS ... [more]
SCV-Nano - 2/20 | Nanotechnology: A Report from the Entrepreneur’s Front Line - starting and financing a venture ... [more]
SCV-Mag - 2/20 | Spin-Transfer Torque RAM (STT-RAM) Technology - an exciting path for realizing Gbit-scale memory ... [more]
SCV-EMB - 2/21 | It’s All About The Timing... Echo Cardiogram Enhancement Through ECG/EKG Triggering ... [more]
SVEC - 2/22 | Engineers Week Banquet & Program - Hall of Fame inductees, celebration of engineering ... [more]
SCV-EDS - 2/23 | Recent Advances in Nanoscale Semiconductor Devices and Process Technologies - half-day colloquium ... [more]
SCV-SSC - 3/12 | 2006 ITRS Overview - The Final Edition - with manufacturing technology guidance ... [more]
SCV-Mag - 3/20 | Magnetic Nanoparticles: Self-Assembly and Nanoscale Behavior - organic solvents, field gradients ... [more]
SCV-SSC - 3/22 | Rethinking Analog: Digitally Driven Analog Design - new research program at Stanford ... [more]

Professional Skills Courses
“Speed Reading for Engineers” Exar, Fremont, February 1 [more]
“Clear Business, Technical, and E-mail Writing” Cypress Semiconductor, San Jose, February 22 [more]
“Budgeting Essentials for Engineers” Exar, Fremont, February 27 (half day) [more]
“Presentation Skills for Engineers” VeriSign, Mountain View, February 28 [more]
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SCV-Mag - 3/20 | Magnetic Nanoparticles: Self-Assembly and Nanoscale Behavior - organic solvents, field gradients ... [more]
SCV-SSC - 3/22 | Rethinking Analog: Digitally Driven Analog Design - new research program at Stanford ... [more]

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From the editor . . .

February is a month of celebration! Yes, there are lots of good reasons – days are getting longer so spring should be on the way. Our Chapters, freshened with new officers and recommitted to serving our local community of engineers, is planning programs for the first half of the year.

But I wanted to call your attention to National Engineers’ Week from February 18 thru 24. Events and publicity during this week bring focus to the exciting developments and proud achievements that we’ve accomplished over the years.

For a bit of perspective on the contributions of engineers, go to the National Engineers’ Week website [www.eweek.org] and click on “50 Engineers You Should Meet”. You’ll find a profile of our own Ray Dolby, a local boy (Stanford) who did a lot to improve the quality of the sounds we hear. Or read about Lei-Kun Cheow in Singapore, how she decided to be an engineer, and what she’s doing to optimize LED production. Check out the dozens of other trend-setters in our profession.

Would you like to see local “heroes” in person? Come to the SVEC Engineers’ Week banquet on Thursday, February 22nd. Mingle with past Hall of Fame members at the reception. This year’s distinguished Hall of Fame inductees will include Dr. Paul Baran, Chairman of NovoVentures (inventor of digital packet-switching), Dr. Bradford W. Parkinson, Professor Emeritus, Stanford University (chief architect of GPS), and Dr. James Spilker, Jr., Consulting Professor, Electrical Engineering & Aeronautics/Astronautics, Stanford University (co-architect of GPS, Co-founder of Loral Space and Communications). Keynote speaker will be Dr. T. J. Rodgers, Founder, President and CEO, Cypress Semiconductor.

Celebrate some of the most outstanding accomplishments in the valley -- discounted tickets through Feb 5!

Paul Wesling, Editor

NOTE: This PDF version of the IEEE GRID – the GRID.pdf – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: www.e-GRID.net
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The twenty-third annual SEMI-THERM Symposium is an international forum dedicated to the thermal design and characterization of electronic components and systems. The symposium fosters the exchange of knowledge between practitioners and leading experts from industry and academia from around the world.

**SHORT COURSES**
- **Thermal Management in Practice: Sense, Nonsense, and Things That Go Wrong** – Robert Moffat, Stanford University, USA; Clemens Lasance, Philips Research Laboratories, The Netherlands
- **Employing the Latest Innovative Technologies in Present and Future Electronic Products** – Gamal Refai-Ahmed, AMD Inc.; Prof. Dereje Agonafer, University of Texas, Arlington; Bahgat Sammakia, Binghamton University
- **Excel Power: Tips and Tricks for Thermal Calculations and a Whole Lot More** – Cathy Biber, Biber Thermal

**SESSIONS**
- Electronics Packaging Characterization
- System Level Analysis
- Die Level Thermal Management
- Developments in Liquid Cooling
- Thermal Interface Materials: Characterization and Uses
- Conduction and Thermal Spreading
- Advances in Air Cooling
- Modeling and Simulation in Thermal Management
- plus poster sessions, embedded tutorial

**EXHIBITS AND VENDOR WORKSHOPS**
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The International Symposium on Code Generation and Optimization (CGO) provides a premier venue to bring together researchers and practitioners working on feedback-directed optimization and back-end compilation techniques. The conference covers optimization for parallelism, performance, power, and security, where that optimization occurs in the mapping from an input (including APIs, high-level languages, byte codes such as .NET or Java, or ISAs) to a similar or lower-level target machine representation.

**Workshops**
- Optimizations for DSP and Embedded Systems
- Software Tools for Multi-Core Systems
- EPIC Architectures and Compiler Technology
- Data-Parallel Programming for Many-Core Architectures

**Tutorials**
- Practical Phoenix: A Hands-On Tutorial
- GCC Internals
- Open64: the Open Source High-Performance Compiler

**Topical Areas**
- Compilers, back-end code generators, translators
- Binary optimization tools and techniques
- Profiling and feedback-directed methodologies
- Innovative analysis, transformation, and optimization techniques
- Intermediate representations for powerful or efficient optimization
- Vertical integration of language features, representations, optimizations, and runtime support for parallelism
- Thread extraction and thread-level speculation
- Phase detection and analysis techniques
- Mechanisms and optimization techniques for efficient security protection models
- Traditional compiler optimizations

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San Jose State University
One Washington Square
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For more information about the Electrical Engineering Department, visit www.engr.sjsu.edu/electrical
RSA® Conference helps drive the information security agenda worldwide with annual events in the U.S., Europe and Japan. Over its 16 year history, it has consistently attracted the world’s best and brightest in the field, creating opportunities for conference attendees to learn about information security’s most important issues – through first-hand interactions with peers, luminaries and both emerging and established companies. RSA Conference delivers knowledge, best practices, insight, perspective and unequalled opportunities to connect and collaborate, as the most respected, highly attended, and eagerly anticipated information security event in the industry.

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Pre-Conference 1- and 2-Day Tutorials
(Sun and Mon, Feb. 4 and 5) Partial listing:
- Secure Web Services
- Exploitation: 0-60 in 3.5
- Defending VoIP Networks
- Web Application Security Workshop
- Emerging Smart Card API and Interoperability Standard
- Smart Cards in IT: Issuance, Management, and Usage
- Smart Cards in IT: Putting Smart Cards into Action
- Creative Web Protocol Attacks, Beyond Web Hacking
- Proven Performance Penetration Testing
- Side-Channel Attacks: Intro to Timing Attacks, SPA, and DPA
- How Do You Make Cryptography Work in the Real World?
- Infrastructure Attacktecs & Defentecs: Hacking Cisco Networks
- Analyzing Wireless Security
- Learning to Speak Crypto
- Authentication Evolution

Keynote Speakers
Bill Gates, Chairman, Microsoft Corporation
Craig Mundie, Chief Research and Strategy Officer, Microsoft Corporation
Larry Ellison, CEO, Oracle Corporation
John Thompson, Chairman and CEO, Symantec Corp.
Stratton Sclavos, Chairman, President and CEO, VeriSign
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- The U.S. Department of Defense’s Director of Defense Manpower Data Center

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- Ed Chan, Director of Security, Tivo Inc.

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Keynote Address:
Al Gore, “The Democratization of Technology”
Tues April 3, 11 AM – Noon

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Moderated free-form discussions for swapping ideas with your peers on common embedded development problems.

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Wednesday, April 4, 7:00 – 10:00PM at the Tech Museum

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Prius Teardowns
We will tear apart and look at the electronics in a Toyota Prius (yes really tear apart!) and a number of other cool products that are pushing the boundaries of system design.

The Disruption Zone
Hear from software and hardware companies seeking to change forever the embedded systems industry through revolutionary technologies – new business models, 10x improvements & more.

Register now to ensure your participation!

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The Embedded Systems exhibits floor features leading companies showcasing cutting-edge hardware, software, tools, and the full spectrum of system components. You will learn relevant new skills, meet and talk with vendors, network with peers, and develop new strategic partnerships – all under one roof, at one time, with both daytime and evening hours:

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The International Symposium on Quality Electronic Design (ISQED) is a premier Manufacturing, Design, and Design Automation conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading conference dealing with design for manufacturability and quality issues front-to-back. The conference attendees are primarily designers of the VLSI circuits & systems (IP & SoC), process/device technologists, semiconductor manufacturing specialists including equipment vendors, and those involved in the R&D and application of EDA Tools & design flows. ISQED emphasizes a holistic approach toward design quality and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities. The conference spans three days, Monday through Wednesday, in three parallel tracks, hosting over 100 technical papers, six keynote speakers, two panel discussions, workshops /tutorials and other informal meetings. ISQED proceedings are published by IEEE Computer Society and hosted in the digital library. Proceedings CD ROMs are published by ACM.

CONFERENCE HIGHLIGHTS

TUTORIALS/WORKSHOPS
ISQED 2007 is pleased to offer a single full-day tutorial track, presented by several experts in their respective fields. This tutorial track consists of several major topics such as Emerging Nano Devices and Low-Power Design, Role of Bioelectronics for Quality of Life, Energy-performance-variability Trade-offs, Advanced modeling of analog and mixed-IC circuits, and Design Methodologies and Tools for Circuit Design in CMOS Nanometer Technologies.

Emerging Circuits, Power, and Variability Tolerant Design
Multi-Gate MOSFET Design: Gerhard Knoblinger, Infineon Technology
Sub 45nm Low Power Design Challenges: James W. Tschanz, Intel
Self-Adaptive Systems to Drive out the Nano-scale Devil: Marcal Pol, IMEC

PLENARY SESSIONS
Two plenary sessions will be held on Tuesday and Wednesday mornings. Several industry & academia leaders will discuss the issues surrounding electronic design, design for yield and manufacturability and other critical topics from various points of view. Plenary keynote speakers are:

Jeong-Taek Kong, Vice President, Samsung, Korea
Joe Sawicki, GM and VP, Mentor Graphics, USA
Marc Duranton, Principal Scientist, NXP Semiconductors
Philippe Prous, Gemalto, France

LUNCHEON SPEECH
How Can Designers Ensure the Quality of Their IC Designs at 65 and 45 Nanometers? Antun Domic, GM and VP, Synops

DFM, DFT and SOC
DFM and Yield: Srikanth Venkataraman, Intel
DFT, Test, Debug and Diagnosis: N. Nagapalli , AMD
Quality-driven Architecture Synthesis and Power Aware Design of Embedded SoCs: Dr. Lech Jozwiak, Eindhoven U. of Technology

PANEL DISCUSSIONS
ISQED is pleased to offer two high-power evening panel discussion sessions, where many leading experts address the important issue of quality design. These panels would focus on the following topics:

1. DFM: EDA’s salvation or its excuse for being out of touch with engineering?
2. Do Digital Design and Variability Mix Like Oil and Water?

VENDOR EXHIBITION
After a successful start in 2006, the 2nd ISQED exhibition is being held in conjunction with ISQED07, features vendors offering design tools and methodologies in the area of design for manufacturing and quality. The exhibit floor will be open on Tuesday March 27, in parallel with technical sessions.

TECHNICAL SESSIONS
ISQED Technical sessions start on Tuesday March 27, and continue until the afternoon of Wednesday, March 28. Beside the above plenary sessions, panel discussions, and workshops, the program consists of nineteen technical sessions featuring over 100 papers on various challenging topics related to design for manufacturability and quality. A partial list of topics is shown below. Detail program would be available on the web at www.isqed.org.

EDA Methodologies, Tools, Flows & IP Cores; Interoperability and Reuse (EDA)
Design for Manufacturability & Quality (DFMQ)
Design Verification and Design for Testability (DVFT)
Package - IC Design Interactions & Co-Design (PDI)
Design of Reliable Circuits and Systems (DFR)

Robust Device, Interconnect, and Circuits (RDIC)
Physical Design, Methodologies & Tools (PDM)
Emerging/Innovative Process & Device Technologies and Design Issues (EDT)
System Level Design, Methodologies and Tools (SDM)

REGISTRATION
Please refer to the ISQED web site at www.isqed.org for information regarding the tutorials, conference, and hotel registration. Direct all conference inquiries to isqed@isqed.org. Early registration is recommended to take advantage of the discounted fee through March 14th.

FEBRUARY 2007 Visit us at www.e-GRID.net
For more than a decade, DesignCon has delivered technical content and practical solutions for enhancing your designs, backed with the assurance of industry expertise. The 2007 lineup again draws out the industry's best advances affecting design engineers.

Exhibits feature leading organizations presenting EDA tools, test and measurement equipment, PCBs and related technologies, semiconductor components and IP, interconnect technologies, and more. Papers discuss leading-edge case studies, technology innovations, practical techniques, design tips and application overviews.

Technical tracks:
- Chip-Level Functional Design
- Chip-Level Physical Design and Verification
- Power and Package Co-Design
- PCB, Package, and Passive Technologies
- Chip and Board Interconnect Design
- High-Performance Backplane Interconnect Design
- High-Speed Timing, Jitter and Noise
- Power Integrity
- Functional Verification
- Business Issues

Technical Panels:
- Jitter and Its Challenges when Testing Serial Data Designs
- Controlled-ESR Bypass Capacitors: Myths and Truths
- Best Design Practice for High-Speed Serial Links
- Emerging Challenges of DC-DC Converters
- Selecting the Right Encryption for Securing Silicon IP
- Who Verifies Your Third-Party Design IP?
- … and more

Keynote Speakers:
- Steve Polzin, Senior Fellow and Chief Platform Architect, AMD
- Willem P. "Wim" Roelandts, CEO & Board Chairman, Xilinx
- Leah Jamieson, IEEE President & Dean of Engng, Purdue Univ.

Business Forum Panels:
- Keeping It Cool: Strategies and Considerations for Dealing with Thermal Performance
- Putting the "D" Back into DFM
- Life Begins at 65 – Especially for Mixed Signal
- Embedded Memory Needs & Options for Consumer Products
- The Business Impact of IP Quality on Market Growth
- DFM: Can Designers Afford NOT to Do It at 65 nm?
- … and more

Discover the latest tools and methods to overcome your design challenges and drive tomorrow’s innovations at DesignCon 2007. Semiconductor and electronic design engineers will find the right mix of technical education and networking opportunities, with access to cutting-edge design products.
IEEE Professional Skills Courses

Breakthrough Project Management
Date/Time: Tues & Wed, January 30-31, 8:30 AM – 4:30 PM
- Location: TIBCO Software, Palo Alto
- Fee: $600 for IEEE Members; $675 non-members

Speed Reading
- Date/Time: Thurs, February 1, 8:30 AM – 3:30 PM
- Location: Exar, Fremont
- Fee: $375 for IEEE Members; $450 non-members

Budgeting Essentials for Engineers
- Date/Time: Tuesday, Feb. 27, 8:30 AM – 12:30 PM
- Location: Exar, Fremont
- Fee: $275 for IEEE Members; $325 non-members

Presentation Skills for Engineers
- Date/Time: Wed, Feb 28, 9:00 AM – 5:00 PM
- Location: VeriSign, Mountain View
- Fee: $450 for IEEE Members; $525 non-members

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Preparing Technical Presentations for Management
- Date/Time: Tues, March 6, 8:30 AM – 4:30 PM
- Location: Sybase, Inc., Dublin
- Fee: $375 for IEEE Members; $450 non-members

Transitioning from Individual Contributor to Manager
- Date/Time: Wed, March 7, 8:30 AM – 4:30 PM
- Location: TIBCO Software, Palo Alto
- Fee: $375 for IEEE Members; $450 non-members

Improve your skills – register for one of these classes, or for others coming up this spring. Bring a team!

For complete course information, schedule, and registration form, see our website:

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First IEEE International Workshop on Safety of Systems
Mar. 15-16, 2007
Naval Postgraduate School, Monterey

The newly created Technical Committee on System Safety under the IEEE Systems Council invites you to the first annual international workshop on issues relating to safety of systems of national and global significance. The purpose is to provide an open working forum to contribute to the goal of obtaining a holistic view of system safety for a better understanding of the system safety discipline. It will examine the overlap and interdependencies among related safety, complexity, reliability, dependability and security engineering technical communities across civil, commercial and defense sectors. Because IEEE technical societies contain expertise in various slices of the discipline of system safety, obtaining both the big picture and coordination among the separate initiatives is difficult to achieve in any one specific society. This workshop aims to become a unique integrating forum for researchers and practitioners to discuss the practical issues associated with safety of systems.

Topics addressed at IWSS’07:
- Safety engineering of systems-of-systems
- Building a safety culture and management of safety
- Safety Standards and Ethics
- Competency of safety practitioners
- Human factors and ergonomics
- Development of the safety requirements to identify the safety functions to be performed and identification of the safety integrity of the various safety functions
- Hazard analysis and risk assessment techniques for development of the safety requirements specification
- Design and implementation considerations
- Modeling and formal methods of assurance
- Effective and appropriate use of tools
- Assessment of safety and development of safety cases
- Education and teaching materials

Position papers are accepted through Wednesday, January 31

More details in the Call for Papers:

www.ieeesystemscouncil.org
Consumer Electronics Show Download

Speakers: the Chapter officers and others
Time:  pizza and drinks at 6:00 PM;
       Presentations at 7:00 PM
Cost:  $5 for members, $10 for non-members
Place:  Oak Room at Hewlett-Packard, 19447
       Pruneridge Avenue (Building 48 at Wolfe
       and Pruneridge), Cupertino
RSVP:  not required
Web:  ewh.ieee.org/r6/scv/ce

Come and find out what might be happening in consumer electronics during 2007 and beyond. Some of the attendees at the recent Consumer Electronics Show (CES) in Las Vegas will give you their analysis of “what's hot” in Wireless/Mobile, Game Consoles, UPC, Display Technology, Digital Imaging, Storage, and a lot more. There'll also be a summary of the co-located ICCE Conference.

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Best of ISTFA: Highlights from the Int'l Symposium for Testing and Failure Analysis

Speakers: various attendees of ISTFA
Time: 6:30 PM: social and refreshments; 7:00 PM Presentation
Cost: none
Place: HP Oak Room, Bldg 48, Pruneridge Ave. at Wolfe Road, Cupertino
RSVP: not required
Web: ewh.ieee.org/r6/scv/rl

The International Symposium for Testing and Failure Analysis (ISTFA) provides a forum for the latest developments in wafer, chip, package, and board-level test and failure analysis. The 29th ISTFA was held November 12-16, 2006, in Austin. Information on ISTFA is available on the web at http://www.asminternational.org/istfa/. The January Santa Clara Valley IEEE Reliability Society meeting will feature a panel discussion of selected papers from ISTFA. The panel is being organized by Art Rawers. We are looking for additional panel members, especially ISTFA attendees. If you are interested in helping select papers, being on the panel, leading a discussion, or contributing in another way, please e-mail us at reliability@ieee.org.
Dense wavelength division multiplexed (DWDM) large-scale, single-chip transmitter and receiver photonic integrated circuits (PICs) capable of each operating at 100Gbit/s have been deployed in the field in Infinera Optical Transport Equipment since the end of 2004. These highly integrated InP chips have significantly changed the design and performance of long haul optical transport networks. First, a review of the 10 channel, 100Gbit/s PIC is presented. Then two extensions of the technology are demonstrated; first is the wide temperature, colorless operation of the 100Gbit/s PIC, and secondly a single integrated chip with 40 channels each operating at 40Gbit/s capable of an aggregate data rate of 1.6Tbit/s.

These advances in photonic integration should be viewed in light of what is otherwise commercially available; single channel transmitters with up to 6 elements to provide for wavelength tunability and high speed data modulation. In contrast the 10 channel, 100Gbit/s transmitter PIC’s from Infinera currently in deployment have over 50 elements and the 1.6Tbit/s capable transmitter PIC in development has over 240 elements.

He has authored/co-authored over 100 publications in journals and conferences, and three book chapters mainly in the area of high speed optical components.

He is a Fellow of the Optical Society of America (OSA) and a Senior Member of IEEE/LEOS.

Radha Nagarajan obtained his B.Eng. (First Class Honors) degree in Electrical Engineering from the National University of Singapore where he studied under the Government of Singapore Undergraduate Merit Scholarship. He was then awarded the Hitachi Foundation Scholarship to study at the University of Tokyo, Japan, where he obtained his M.Eng. degree in Electronic Engineering. He obtained his Ph.D. in Electrical Engineering from the University of California, Santa Barbara, where he was awarded the General Affiliates Dissertation (Ph.D.) Fellowship. Upon finishing his Ph.D. in the area of carrier transport effects in high speed quantum well lasers, Radha Nagarajan spent two years as a research faculty at the University of California, Santa Barbara, working on, among other things, microwave fiber optic links. He subsequently joined SDL in 1995. He first worked on the development of high speed fiber optic links for wide temperature range operation (-55°C to 125°C) in space and other harsh environments. He later managed the development of the new generation high power, 980nm single mode pump modules for EDFA applications. The 300mW pump module won the Photonics Circle of Excellence Award in 2000. At the time of being acquired by JDS Uniphase, he was a Senior Manager with the Advanced Technology Group working on the development of next generation high speed optical components. In May 2001, he joined Infinera in Sunnyvale, CA, where he is currently the Director of Advanced Development for photonic integrated circuits.
Recipe for a New Embedded Component: Connectors

Speakers: Dirk Brown and John Williams, Neoconix
Time: 6:30 PM dinner (optional); 7:30 PM Presentation
Cost: Seated dinner served at 6:30 - $25 if reserved before Feb 11; $30 after & at door
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road near Lawrence Expy), Sunnyvale
RSVP: through PayPal on website, or by email to Janis Karklins, karklins@ieee.org
Web: www.cpmt.org/scv

Neoconix’ (neoconix.com) roots go back to AMD’s Submicron Development Center in the mid-1990’s. Two engineers, Dr. Dirk Brown and John Williams, working together on chip-level interconnects, realized that many of the system performance bottlenecks were occurring at the packaging and PWB level.

The pair went to Cornell University to join a company called HCD that was working on novel connector and PWB technologies. HCD’s CEO, Professor Che-Yu Li, was a renowned interconnect and packaging expert and had previously mentored Dirk for his Ph.D in materials science at Cornell.

Dirk ran sales and marketing while John took charge of engineering and manufacturing for HCD, leading to proprietary design wins and licensing deals with some of the largest semiconductor and electronics manufacturers in the industry.

In early 2003, Dirk and John founded the forerunner of Neoconix, based on an inspiration that merges the worlds of printed circuit fabrication, chemical milling, and connectors.

Connectors and sockets as we know them today are assemblies of stamped metal contacts housed in a molded plastic part. Neoconix uses photolithography, potentially offering better dimensional scalability and resulting electrical performance improvements, plus lower cost. The implications of the Neoconix technologies are nothing less than a complete shift of today’s interconnection paradigm. Low-profile connectors – about as thick as a printed circuit – are just what portable products need.

Recipe for a New Embedded Component—Connectors: Fabricate rigid or flexible printed circuit boards and chem mill contact sheets. Form and plate the contacts and etch them apart after insertion between pre-drilled printed circuit layers and press.

In summary, here are some of the results:

- A concentration on land grid array connections today, that takes advantage of fine dimensions, low parasitics, good contact wipe (and major customer needs)
- The ability to circuitize the board, embed discrete or distributed bypass capacitors and terminating resistors
- Differentiate dense contacts by high resolution photolithography etched apart into signal, ground, and voltage — no piece-parts to individually plate or assemble
- Overcome the scaling-down disadvantages of stamp-and-form by use of photolithography and etch

The technology is particularly appropriate for the low profile requirements of flex circuit connectors, and the implications of the Neoconix technologies are nothing less than a complete shift of today’s interconnection paradigm, including a whole new way of making connectors.

Embedded connectors will give new freedom to designers to design their connectors integral with systems, wherever they want them. It’s a supply chain simplification.
Impedance Matching Networks and Fundamental Limits

Speaker: Steve Stearns, Senior Staff Engineer, Northrop Grumman Mission Systems
Time: 6:00 PM Social time; 6:30 PM Presentation
Cost: none
Place: National Semiconductor Bldg #9, Classroom #4, 2900 Semiconductor Dr., Santa Clara
RSVP: not required
Web: www.mtt-scv.org

Impedance-matching problems are divided traditionally into three distinct categories ranging from simple to hard. These are single-frequency matching, multiple-frequency matching, and broadband matching. In all cases, design algorithms for passive lossless match networks have been developed. These algorithms are explained easily on a Smith chart and can be carried out manually. However, broadband impedance matching, unlike single-frequency and multiple-frequency matching, is subject to a fundamental limitation. Network synthesis theory yielded a remarkable theorem, proved by R.M. Fano in 1947, that bounds the return-loss match-bandwidth product of all passive, lossless impedance-matching networks regardless of complexity. The speaker will present two surprising strategies that enable one to evade the Fano bound and achieve apparently impossible results. These strategies lead to two classes of impedance matching networks (one old, one new) with extreme performance claims and distinct engineering challenges.

Steve Stearns is Senior Staff Engineer at Northrop Grumman Mission Systems (formerly TRW), Electromagnetic Systems Laboratory, in San Jose. He previously held positions as Senior Scientist at Technology for Communications International, Senior Member of the Technical Staff at GTE Government Systems Corporation in Mountain View, as well as Probe Systems Inc. in Sunnyvale, and Hughes Aircraft Company Ground Systems in Fullerton. Steve attended California State University Fullerton, the University of Southern California, and Stanford University. He is a Senior Member of the IEEE, has over 50 publications and presentations, and has eight U.S. patents and numerous foreign patents. He holds two federal FCC licenses: Amateur Extra class and commercial General Radio Operator with Radar Endorsement. He writes a column on topics in electromagnetics and antennas, and serves as a reviewer for an IEEE Transactions journal.
A/D and D/A Converters with Integrated High-speed Compression

Speaker: Al Wegener, CTO, Samplify Systems, Inc
Time: 6:30 PM Pizza and social; 7:00 PM Presentation
Cost: $1 for food
Place: National Semiconductor, north end of Building E, 2900 Semiconductor Dr., Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/sps

Al Wegener is the founder and CTO of Samplify Systems, a venture-funded start-up whose patented compression solutions reduce bandwidth and storage bottlenecks in sampled data systems. Mr. Wegener is a DSP engineer, technical manager, and inventor with more than 25 years of experience in defense electronics, professional and consumer audio, and wireless applications. Mr. Wegener founded Samplify Systems to bring the benefits of high-speed lossless and lossy compression to signal processing systems at sampling rates above 10 Msamp/sec, where no effective compression solutions were previously available. Prior to Samplify Systems' first venture funding, Mr. Wegener was the technical manager of Texas Instruments' Palo Alto ASIC design center (formerly Graychip), where he was the project lead and chip evangelist for the GC1115 crest factor reduction processor. Mr. Wegener holds a BSEE from Bucknell University and an MSCS from Stanford University. Mr. Wegener holds nine issued U. S. patents and is named on seven additional, pending Samplify Systems patents.

Various compression methods have become integral components of computer systems (WinZIP), audio distribution (MP3), and video processing (MPEG, H.264). However, effective and efficient compression techniques for high-speed A/D and D/A converters have not been available. This talk describes the Samplify series of algorithms, which provides both lossless and lossy compression of bandlimited, sampled data acquired by A/D converters, or provided to D/A converters, and then further processed by FPGAs or ASICs. Samplify provides a lossless compression mode whose compressed data rate varies, depending on the redundancy present in the signal. Samplify also offers two complementary lossy compression modes, in which users select either a desired compression ratio (such as 2.05:1 or 3.68:1) or a desired dynamic range (such as 65.5 dB). Examples using common, bandlimited signals demonstrate the rate-distortion tradeoffs enabled by the Samplify algorithms. Improved compression ratios can be achieved by combining a training phase, in which the signal’s characteristics are discovered, with a compression phase. The Samplify algorithms require a modest amount of FPGA resources and operate at up to 200 Msamp/sec. Higher sample rates are achieved by instantiating parallel compression and decompression blocks.
Recent Progress in Photovoltaics - An IMEC View

Speaker: Dr. Robert Mertens, IMEC, Belgium
Time: 6:15 PM Pizza and social; 6:15 PM Presentation
Cost: none
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/upcoming-events.html

Robert P. Mertens received the Electrical Engineering (MSEE) and Ph.D. degrees from the Catholic University of Leuven, Belgium, in 1969 and 1972 respectively. He was a visiting scientist at the University of Florida in 1973.

After his return to Belgium in 1974, he became a senior research associate of the National Foundation for Scientific Research of Belgium.

In 1984 he joined the Interuniversity Microelectronics Center (IMEC) as research manager for materials research and packaging. Until December 2006, he was the Senior Vice President of IMEC for Micro-Systems, Components, and Packaging.

Today he is an IMEC Senior Fellow and Senior Vice President for IMEC’s Scientific Leadership team. Since 1984 he has been a professor at the University of Leuven, where he is teaching courses on semiconductor devices and on the technology of electronic and optoelectronic systems.

He was elected Fellow of the IEEE for contributions to heavily-doped semiconductors, bipolar transistors, and silicon solar cells. He has authored or co-authored more than 300 publications, has received several best paper awards, and has been program chair of several technical conferences.

The European vision on the cost and market evolution of photovoltaics will be explained. The solar cell roadmap of IMEC will be presented. The IMEC work on crystalline silicon and organic cells will be covered.

In the field of wafer-based industrial crystalline silicon cells, an evolutionary path towards thinner and therefore cheaper cells will be highlighted. Efficient epitaxially grown silicon solar cells and very thin (5 mm thick) crystalline silicon cells on glass or ceramic substrates will be discussed. These very thin cells are based on a lift-off approach or an aluminum-induced crystallization.

In organic solar cells, IMEC is concentrating on bulk donor-acceptor heterojunctions based on P3HT:PCBM for which state-of-the-art results, ie. an efficiency of 4.3 percent, will be reported. The importance of the blend ratio and the kind of solvent used will be illustrated in the talk.
Numerical simulations for EMC applications have been proven to be very cost effective when comparing different design options. Different EMC design practices such as minimizing coupling paths, shielding, grounding practices and filtering can be effectively evaluated using numerical simulations. In most EMC applications the geometry and the complexity of the problem needs to be highly simplified in order to achieve a model that can be computed within a reasonable amount of time and memory. In this talk, this simplification process will be shown using models of common real-world EMC applications. The simulation results will then be compared to measurements to validate the process. The examples presented will show how the visualization of EM fields and currents allows engineers to have an insight of the system, to suggest design alternatives and to quantify in advance the effectiveness of each different solution.

Federico Pio Centola received his Laurea degree in electrical engineering from the University of L’Aquila, Italy in 2001 and the M.S. degree in electrical engineering from the University of Missouri Rolla in 2003. From 2001 to 2003 he has been with the Electromagnetic Compatibility Laboratory at the University of Missouri Rolla where he was a visiting scholar and a graduate research assistant. His research interests included numerical simulations, electrostatic discharge and shielding.

He has been an EMC instructor and consultant for Flomerics Inc. where he specialized in applying numerical simulations to solve EMC problems. He is currently working for Flomerics as an Electromagnetic Application Engineer.
Sean Murphy has taken an entrepreneurial approach to life since he could drive. He has served as an advisor to dozens of startups, helping them explore new options and bring their businesses to new levels. His firm, SKMurphy, Inc., focuses on early customers and early revenue for software startups, helping engineers to understand business development.

Prior to SKMurphy, Sean worked in a variety of areas including software engineering, engineering management, application engineering, business development, product marketing and customer support. His clients include Cisco Systems, 3Com, AMD, MMC Networks, Escalade and VLSI Technology. Sean holds a BS in Mathematical Sciences and an MS in Engineering-Economic Systems from Stanford University.

Blogs and wikis are two "new" social software technologies that have been deployed in production use now for more than a decade. Learn at least ten tips about the practical benefits of adding a blog to your website, using blogs for project communication, and wikis for project coordination and collaboration. If you, your prospects or your clients are relying on an email inbox as the primary filing system for keeping a project organized (e.g., "who has the most current version of this project document?"), this talk will provide insight on new ways to get your proposals accepted and your final work signed off for payment.

Does your client keep revisiting the same decisions? This talk will offer tips on how blogs and wikis can cut the time needed to reach consensus on project deliverables when a deadline looms. You will leave with a practical understanding of usage models that leverage the distinct strengths of these tools for both landing new projects and collaborating with your customers and partners to create project deliverables. Learn the practical benefits of using a blog for project communication and a wiki for project coordination and collaboration, and how to use these tools to land new projects and create deliverables.
The February 15th meeting of the Industry Applications Society for Oakland East Bay Section will feature a talk entitled "Short Circuit Current Rating of Industrial Control Panels". The speaker will be Bob Roy, Technical Sales Engineer, Cooper Bussmann. Here is an outline of the topics that will be covered:

- Definition of Short Circuit Current Rating and Interrupting Rating
- Video on Interrupting Rating
- 2005 NEC Code requirements for SCCR in Articles 230, 409, 430, 440, and 670
- U.L 508 Supplement SB Method for determining SCCR's
- Example: SCCR control panel

Our speaker is Bob Roy, Technical Sales Engineer, Cooper Bussmann. Bob received his BS in Electrical Engineering at the University of Tennessee. He has worked for Cooper Bussmann as Technical Sales Engineer for 14 years. Bob has also worked for Kaiser Engineers, General Electric Supply Co., Pacific Gas and Electric Company.
RF ESD Protection Strategies – Design and Performance Trade-off Challenges

Speaker: Dr. Philippe Jansen, IMEC
Time: Refreshments at 6:00 PM, Presentation at 6:30 PM
Cost: Donation to partially cover food costs
Place: National Semiconductor, Building E Auditorium, 2900 Semiconductor Dr., Sunnyvale
RSVP: by email to ssc_scv_rsvp@yahooogroups.com
Web: www.ewh.ieee.org/r6/scv/ssc

Philippe Jansen received his M.Sc. and Ph. D. in electrical engineering from K.U.Leuven, Belgium in collaboration with IMEC in 1988 and 1993 respectively. He performed a post-doctoral research at Hitachi's Central Research Laboratory in Tokyo, Japan. Since 1994, he has worked for IMEC on various topics: advanced CMOS and BiCMOS integration, electrostatic discharge (ESD) protection and advanced packaging. Currently, his interests are in advanced BiCMOS process integration, ESD protection for RF circuits and integrated packaging research and development. Moreover, he is in charge of the IMEC business development office in the US.

Emergence of extensive applications for portable electronics has fueled the rapid deployment of CMOS and BiCMOS based integrated RF front-ends. These technologies demonstrated transit frequencies well above 150 GHz, e.g., with transistors in a typical 90nm CMOS technology, and are commercially available for manufacturing. On the other hand, implementing Electrostatic Discharge (ESD) protection on these RF front-ends designs, such as Low Noise Amplifiers (LNA), is essential to ensure reliable operation. The ESD protection strategies for RF circuits reported in the literature include, but are not limited to classical diodes with power clamps, inductors with power clamp, distributed ESD protection using transmission lines or coplanar wave guides, resonant and cancellation methods and ESD-RF co-design techniques. All these techniques, except the first one, mark a paradigm shift in the ESD protection strategies specifically for high frequency circuit applications. It is also important to note that the protection strategies described above may not be useable in all cases and only a few reports show silicon validation data, especially for sub-130nm technologies. This presentation presents the results of a thorough investigation carried out on four ESD protection strategies in CMOS and BiCMOS technologies to obtain a clear understanding of the possible trade-offs in both RF and ESD design. This is achieved through design and evaluation of RF and ESD performances for a generic LNA, in which the RF pin is protected using different ESD protection approaches.
Dr. Paul Dennig is the chief technology strategist at Ahwahnee, assessing technological trends and market requirements to author key product specifications. He’s also the chief product architect and drives the long-range direction of research and development. He is a veteran of both the semiconductor and hard disk industries, experienced in product and process design, R&D, and manufacturing. Prior to his present position, Dr. Dennig worked for IBM and Hitachi, where he drove strategic roadmaps for new components. He holds a Bachelor’s degree in Electrical Engineering from MIT, a Ph.D. in Materials Science and Engineering from Stanford University, and did post-doctoral research studies in CVD diamond at the National Institute for Materials Science in Japan.

Dr. Dennig will present his first-hand account entitled, “Nanotechnology: A Report from the Entrepreneur’s Front Line.” This talk will touch on the pulse of the nanotechnology business segment, the process of starting and financing such a business venture, and choices of business focus. The goal will be to provoke further discussions to help entrepreneurs clarify their efforts to launch their next businesses.
Spin-Transfer Torque RAM (STT-RAM) Technology

Dr. Yiming Huai is Co-Founder, Chief Technology Officer and Vice-President of Engineering at Grandis, Inc., the pioneer in Spin-Transfer Torque RAM (STT-RAM) technology. Prior to Grandis, he held various positions, most recently as Senior Thin-Film Director at Read-Rite Corporation, where he led the development and manufacturing of industry-leading spin-valve recording heads for hard disk drives from 1996 to 2002. He previously worked as a Staff Scientist at the Lawrence Livermore National Laboratory (LLNL) on ultra-high density magnetic sensors and as a Post-Doctoral Fellow at the National Research Council in Ottawa, Canada. He received M.S. and Ph.D. degrees, both in Physics, from the University of Montreal in Canada.

Dr Huai has over 20 years’ experience in thin-film materials, processing and devices. He has published over 90 papers in scientific journals, holds 32 patents and has more than 40 patents pending. He has given more than 15 invited talks on STT-RAM technology over the last three years and has served as Conference Chairman/Organizer for major international magnetics conferences and workshops. In 1996, he received the prestigious R&D 100 Reward with his peers for his outstanding work on Ultra-High Density Magnetic Sensors.

Spin-transfer torque writing technology, combined with the newly-observed high tunneling magneto-resistance (>300%) in MgO magnetic tunnel junctions (MTJs), provides an exciting path for realizing Gbit-scale STT-RAM (Spin-Transfer Torque Random Access Memory) with low power consumption, fast operating speed (a few ns), and excellent scalability to future semiconductor technology nodes. I will first describe the physics and mechanisms underlying spin-transfer torque switching (STS) and our experimental results showing spin-transfer switching in MgO MTJ bitcells. The techniques involved in reducing the critical STS current and achieving consistent switching in the nanosecond regime will be presented and discussed, along with recent experimental data. The key advantages of spin-transfer-torque writing technology and the technical issues in commercializing STT-RAM will be highlighted. Finally, the potential applications of STT-RAM in mobile devices, digital consumer electronics and automotive products will be outlined. The excellent intrinsic attributes of STT-RAM are attractive for replacing not only existing non-volatile memory products, but also Random Access Memory (RAM), such as SRAM and DRAM, in wireless and embedded applications.
It's All About The Timing...
Echo Cardiogram Enhancement Through ECG/EKG Triggering

Speaker: Prof. David Rivkin, College of Engineering, Drexel University, and EMBS Distinguished Lecturer
Time: optional dinner with the speaker, Stanford Hospital cafeteria, at 6:15 PM; Presentation at 7:30 PM
Cost: none
Place: Clark Center Auditorium, Stanford Univ (free parking after 4 PM)
RSVP: not required
Web: ewh.ieee.org/r6/scv/embs

Prof. David A. Rivkin, PhD, PE is a professional scientist, engineer and organizational manager with over 20 years of high-tech engineering experience and 15 years of engineering management experience leading some of the world’s top firms. Prof. Rivkin teaches at Drexel Universities College of Engineering on both engineering and management topics worldwide. David is a Distinguished Lecturer with the IEEEs Engineering in Medicine and Biology Society and a Senior Member of the IEEE. He has been a frequent guest speaker on engineering management and high-technology issues at IEEE Instrumentation and Measurement Society meetings, chairs both the Silicon Valley Chapter of the IEEE Instrumentation and Measurement Society and the IEEE IMS Technical Committee 34 "Nanotechnology in Instrumentation and Measurement". David is the IEEE liaison to the International Standards Organizations TC-229 "Nanotechnology Standards" and many other international professional society positions including being an Executive Member of "AdvaMed" the Advanced Medical Technology Association. Dr. Rivkin holds PhDs in Applied Mathematics and Engineering Management and other graduate studies in BioPhysics, BioChemistry and Metrology. Dr. Rivkin holds several patents and has nearly 20 pending in the US and internationally. David holds a Professional Engineers License in South Africa in Electrical Engineering.

Working with NASA scientists, and GE and Philips ultrasound engineers, GCPI developed the first SystemC based ECG/EKG monitoring system on a single FPGA. The module acts as a trigger for Echo Cardiogram and other medical imaging systems to improve image quality by reducing motion between image slices. An overview of the development program, technology used and future directions will be discussed. This presentation is for engineers, physicians and engineering managers, covering technical and business processes. (Download preliminary PowerPoint slides from the website.)
Recent Advances in Nanoscale Semiconductor Devices and Process Technologies

Speakers: leading technology researchers from around the world

Time: Registration at 12:30 PM, Talks from 1:00 PM - 6:00 PM

Cost: no charge

Place: Santa Clara University, Santa Clara

RSVP: By email to Samar Saha, samar@ieee.org or call 650-584-2894

Web: www.ewh.ieee.org/r6/scv/eds/upcoming-events.html

A no-cost half-day IEEE SCV EDS Colloquium will be held on the Santa Clara University campus, Santa Clara. This colloquium is sponsored by the IEEE Electron Devices Society and by the local IEEE SCV Electron Devices Society Chapter.

This symposium will feature an invited list of distinguished Electron Devices Society lecturers. The main focus of the colloquium is to learn about recent advances in the field of nanoscale semiconductor devices and their related process technologies.

The following are a list of the critical questions which will be debated and answered during this special colloquium:

* Can scaling successfully continue to nanoscale dimensions?
* What are the nanoscale device options?
* What are the nanoscale process options?
* What are the nanoscale material options?
* Which semiconductor process technologies will work best?
* How much will the nanoscale device technologies cost?

Light refreshments will be served at the mid-afternoon break.
Radiofest'07 – Amateur Radio, the EE’s Ideal Hobby

Come to RadioFest’07, in Monterey! There will be demonstrations of radio modes, a vendor and public flea market, license exams and radio direction finding contest for kids.

The Naval Postgraduate School Amateur Radio Club K6LY and the IEEE Monterey Bay Subsection are sponsoring this event to promote radio communications to families, school kids, homeschoolers, scouts and of course the Ham Radio community. Prepare in advance to pass the free Amateur Radio license exam, now that no Morse code is required.

Examples of some of the seminars and talks are:

- An Astronaut’s experience on the ISS
- Operating DX in an Iraqi War Zone
- Amateur Radio without the Morse Code Requirement
- Ham Adventures at the Big Sur Marathon
- History of Amateur Radio in CA
- Scouting and Ham Radio
- When Amateur Radio is the only communication.
- plus many demos of digital, HF, packet, GPS and other modes

View the program, directions and other up-to-date info, on the website.
In this presentation, one of the most crucial components – the amplitude modulator – of the envelope elimination and restoration transmitter will be presented and discussed.

Over the past decades, many new modulation schemes have been developed to offer higher data rates and better spectral efficiency for the same bandwidth. These modulation formats present difficulties for the power amplifier because of the statistics of the RF envelope.

Conventional class A amplifiers are inefficient for modulations with high crest factors. Some class AB amplifiers including feed forward and pre-distortion methods do improve non-linearity but contribute to efficiency degradation and higher cost.

Most recent applications include Doherty amplifiers that improve efficiency by a 10% factor. For a Doherty amplifier (an envelope elimination and restoration transmitter), the overhead circuitry and complexity is similar to feed-forward and/or pre-distortion. However, the die size is effectively 6 dB (power rating) smaller than its counterpart, hence the implementation cost is lower.

Performance of an amplitude modulator architecture that enables the potential efficiency/cost advantages will be presented. This amplitude modulator delivers 100 watts into 3 ohms in less than 10 nanoseconds. The voltage gain is 10 and provides voltage control from its input to any voltage from 0 to 28 volts. The bandwidth of this amplitude modulator is greater than 50 MHz and its distortion level is better than -50 dBc.
Building Management Systems – Thinking and Designing "Green"

Speaker: Eugene Gutkin, CEO, IBS
Time: Social at 5:30 PM, Presentation at 6:00 PM, dinner at 7:00 PM
Cost: $20 for dinner (preregister; pay at door)
Place: Sinbad’s Restaurant, Pier 2 The Embarcadero, San Francisco
RSVP: by email to Jack Lin, jlin@sfwater.org
Web: www.e-grid.net/docs/0702-sf-ias.pdf

Our speaker for February is Eugene Gutkin, CEO of IBS. Eugene is a mechanical engineer with 25 years of industry experience working with DDC systems. Prior to starting IBS in 1997, Mr. Gutkin worked in Siemens Building Technologies as technician, engineer and project manager.

There are many reasons to begin thinking "Green" when involved in electrical power design. There's money to be made when designing "Green" - for the consulting engineer and for the building owner. Mr. Gutkin will present solutions for measuring and managing a building's energy savings opportunities. The discussion will focus on the latest software tools, enterprise-level management and control of power systems, Load Shedding, Daylight Harvesting, and other tools for making a building as efficient as possible. Find out how the building owner and the consulting engineer can benefit by working with proven energy savings technology. In short, it's all about information – the better you measure, the better you can manage. Since the utilities are also interested in these systems, we will briefly review the available Utility Rebate programs.

Please join us in welcoming our speaker to San Francisco for what is sure to be an interesting and productive session.
2006 ITRS Overview -
The Final Edition

Speaker: Alan K. Allan, SEMATECH
Time: 6:15 PM Pizza and social; 6:15 PM Presentation
Cost: none
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/upcoming-events.html

An overview of the latest version of the International Technology Roadmap for Semiconductors (ITRS) which was completed in December, 2006 will be given in this talk.

In particular, the following items will be emphasized: the technology trend drivers contained in the 2005/2006 ITRS Executive Summary, selected manufacturing technology guidance issues, and the Overall Roadmap Technology Characteristics (ORTC).

Key grand challenges and potential solutions from some of the 2006 ITRS Technology Working Groups will also be reviewed.

Alan K. Allan is currently a Staff Engineer with the Intel Corporation and a SEMATECH assignee. He obtained his BSEE in 1971 from the University of Colorado, Boulder, CO and spent seven years at Motorola Semiconductor, followed by 27 years at the Intel Corporation.

His past responsibilities at Intel include Design Engineer, Process Engineer, Applications Engineer, Product Market Engineer, Product Market Manager, Division Sales Training Manager, Corporate Market Research Council Member, SEMATECH assignee, and International SEMATECH/I300I assignee.

Alan is presently assigned as a Staff Engineer for the Intel Technology Manufacturing Group (TMG) External Programs to support the International Technology Roadmap for Semiconductors (ITRS) effort, the International National Electronics Manufacturing Initiative (iNEMI) Roadmap, the SRC FORCe II University Research Programs, and various SEMATECH Member and Supplier Industry Economic Model Projects.

Alan has been an Intel assignee to SEMATECH for the past eight years. He reports directly to Dr. Paolo Gargini, another Intel assignee to SEMATECH. Since 1998, Dr. Gargini has been the Chairman of the International Technology Roadmap for Semiconductors (ITRS).
Magnetic Nanoparticles: Self-Assembly and Nanoscale Behavior

Speaker: Prof. Sara A. Majetich, 2006 IEEE Magnetics Society Distinguished Lecturer, Carnegie Mellon University
Time: Cookies & Conversation at 7:30 PM, Presentation at 8:00 PM
Cost: none
Place: KOMAG, 1710 Automation Parkway, San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/mag

Dr. Sara Majetich received her A.B. degree in chemistry at Princeton University, and a Masters Degree in Physical Chemistry at Columbia University. Her Ph.D. was in Solid State Physics from the University of Georgia, and following that she did postdoctoral work at Cornell University. She has been a faculty member in the Physics Department at Carnegie Mellon University since 1990 and is now a full professor there. Her awards include the Ashkin Award for excellence in teaching, the Carnegie Mellon University Undergraduate Advising Award, and a National Young Investigator Award from the National Science Foundation. She has three patents and over 100 publications. Her research interests focus on magnetic nanoparticles and nanocomposites and their applications.

The magnetic behavior of a monodomain nanoparticle was first described by Stoner and Wohlfarth nearly sixty years ago, yet this simple system is frequently invoked in discussions of high-density magnetic recording media, magnetic refrigeration materials, and a host of biomagnetic applications. Here we will examine two cross-cutting themes of current research on magnetic nanoparticles: self-assembly and nanoscale magnetic behavior.

Different types of superstructure can be self-assembled from the same type of particles. In organic solvents, two-dimensional arrays with long-range order can be formed using Langmuir layer techniques. These monolayers are also used as nanomasks for crystallographically oriented thin films, which provide an alternative approach to preparing nanoparticle arrays for data storage media. Faceted three-dimensional single “grain” nanoparticle crystals are formed by colloidal crystallization methods. Magnetic field gradients can also be used to guide self-assembly. For example, gold-coated iron oxide particles can be used to image self assembly dynamics in aqueous media, in response to patterned magnetic elements, using plasmon scattering and dark field optical microscopy to track single particles.

The ability to make magnetic nanostructures creates a need for new tools that enable us to visualize their magnetization patterns. Small-angle neutron scattering provides average magnetic correlation lengths within three-dimensional assemblies, where correlations of hundreds on nanometers may be present at low temperature. Electron holography shows real-space magnetization patterns of magnetic monolayers, where vortices and transverse domain walls are present as low energy excitations. Scanning probe techniques have the potential for single-particle-per-bit magnetic information storage.
Rethinking Analog: Digitally Driven Analog Design

Speaker: Dr. Mark Horowitz, Stanford University
Time: Refreshments at 6:00 PM, Presentation at 6:30 PM
Cost: Donation to partially cover food costs
Place: National Semiconductor, Building E Auditorium, 2900 Semiconductor Dr., Sunnyvale
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Mark Horowitz is the Associate Vice Provost for Special Programs and the Yahoo! Founders Professor of the School of Engineering at Stanford University, and Chief Scientist at Rambus Inc. He received his BS and MS in Electrical Engineering from MIT in 1978, and his PhD from Stanford in 1984. Dr. Horowitz is the recipient of a 1985 Presidential Young Investigator Award, an IBM Faculty Development Award, the 1993 ISSCC Best Paper Award, the ISCA 2004 Most Influential Paper of 1989, and the 2006 IEEE Solid-State Circuits Award. He is a fellow of IEEE and ACM.

Dr. Horowitz's research area is in digital system design, and he has led a number of processor designs including MIPS-X, one of the first processors to include an on-chip instruction cache; TORCH, a statically-scheduled, superscalar processor that supported speculative execution; and FLASH, a flexible DSM machine. He has also worked in a number of other chip design areas including high-speed and low-power memory design, high-bandwidth interfaces, and fast floating point. In 1990, he took leave from Stanford to help start Rambus Inc, a company designing high-bandwidth memory interface technology. His current research includes multiprocessor design, low power circuits, high-speed links and new graphical interfaces.

As we continue to scale CMOS technology, more chips integrate a small amount of mixed signal circuitry on their large digital dies. Since transistors are getting worse, and the specs for the analog are getting tighter, all these blocks use numerous cheap digital gates to "improve" their analog performance. This talk will discuss a new research program we are starting at Stanford University to try to rethink analog design. The first step is to realize that digital correction is here to stay, and is pretty cheap. So the first research question is can we build mostly "digital" analog subsystems, and are there power/design time advantages in this approach. Since there will be some analog circuitry that remains, the second research question is to try to create a design system that makes using mixed-signal blocks more like using digital macros -- each cell comes with a validation script, and a set electrical rules checkers that ensure the design assumptions are actively checked every time it is used. Our goal in this section is to create robust mixed signal cells that can be used in many different designs. More importantly this tool should provide management feedback on when redesign of an analog cell is really needed, and prevent simple chip errors from reappearing when a new designer redesigns an existing block.