CHAPTER MEETINGS

SCV-LEOS - 8/7 | **Low-Cost Solar Cells Exploiting Silicon Ink Technology** - manufacturing using silicon nanotechnology ... [more]

SCV-EDS - 8/14 | **Unlocking the Potential of Solar Photovoltaics** - state-of-the-art in conversion of sunlight to electricity ... [more]

SCV-SSC - 8/16 | **A Digitally Modulated Polar CMOS PA with 20MHz Signal BW** - high linearity and high power effeciency ... [more]

SCV-Nano - 8/21 | **Today's Scanning Probe Microscopy (SPM) in Nanotechnology: An Introduction** - advanced applications ... [more]

SCV-CE - 8/28 | **WirelessHD: High Bandwidth for Home Entertainment** - what's being planned for your home ... [more]

SPECTRUM - 9/6 | **Multiphysics for MATLAB Users** - one-hour free webinar; build, run, and post-process models directly ... [more]

SCV-EDS - 9/13 | **Nanotechnology, Molecules and the Future of Electronics** - what is real, what is not real in nanoscale ... [more]

SCV-ComSoc/CAS/SPS - 9/17 | **Transceiver Designs for Multicarrier Transmission** - discrete multitone for wired DSL and VDSL, and OFDM for wireless LAN ... [more]

SCV-Mag - 9/18 | **State-of-the-art Ferrite Materials for Fundamental Research, Nano-science, and High-Frequency Applications** - nanoparticles, films, single crystals, metamaterials ... [more]

SCV-CNSV - 9/18 | **Joint Venture Risks** - danger flags, practical ways to minimize risk, suggestions for exclusive licensee risks ... [more]

SPECTRUM - 9/20 | **Leveraging Multiphysics Solutions for Cost-Effective and Successful Electronic Design** - one-hour free webinar, simulating the design of electronic/electromechanical devices ... [more]

SCV-Rel - 9/26 | **Formation of a Warranty Chain Management Institute and its Applicability for Reliability Engineers** - warranty events and costs ... [more]

OEB+SF-PES - 9/27 | **Recent Trends in Substation Automation and Enterprise Data Management** - Intelligent Electronic Device (IED) integration and automation ... [more]

SCV-Mag - 10/16 | **Imaging Magnetic Surfaces with Atomic Resolution** - spin-polarized scanning tunneling microscopy for magnetic nanostructures ... [more]

One-Day Seminars

IT and Materials Technologies from Japan
- Bio Nano Process, Sound, Solar Cells, more
- Tuesday, August 21 - No cost [more]

Broadband and RF Circuit Analysis and Design in CMOS Technology - Saturday Sept 15 – 8:30 AM – 1:00 PM
- Cadence Design Systems, San Jose [more]

Upcoming Conferences

Aug 7-9: **Flash Memory Summit 2007**
- Santa Clara Marriott, Santa Clara [more]

August 21: **IT and Materials Technologies from Japan**
- UC-Santa Cruz Extension, Sunnyvale, free
- Early registration through **August 7** [more]

Sept 5-7: **Energy Nanotechnology Int'l Conference**
- Santa Clara University
- Early Bird rates through **July 30** [more]

Sept 12: **FSA Suppliers Expo & Conference**
- Santa Clara Convention Center
- Complimentary registration through **Sept 7th** [more]

Sept 16-19: **IEEE Custom Integrated Circuits Conf (CICC'07)** - Double Tree Hotel, San Jose
- Early Bird rates through **August 24** [more]

October 8: **OFDM Workshop**
- Santa Clara Univ - Early Bird rates thru **Sept 5** [more]

Oct 25-26: **RoboDevelopment Conference & Expo 2007**
- San Jose Convention Center
- Early Bird rates through **Sept. 14** [more]

Santa Clara University Graduate School of Engineering
Summer Open University Classes [more]

Professional Skills Courses
- **Managing Across Cultures**
- **Presentation Skills**
- **High-Impact Communication**
- **Creative Problem Solving** [more]

Technical Skills Courses (sponsored by SCV Section)
- **PCB Design Fundamentals for Analog and RF**
- **Analog CMOS Integrated Circuit Design**
- **Digital VLSI Design with Verilog**
- **Micro-Electro-Mechanical Systems (MEMS) - Technologies and Opportunities**
- **Design-for-Yield & Design-for-Manufacturing (DFY/DFM) - Principles and Challenges** [more]

Support our advertisers

MARKETPLACE – Services page 3

K-12 Classrooms: Volunteers Needed page 5

IEEE GRID

Your Networking Partner®

August 2007 • *Volume 54 • Number 8*

IEEE-SFBAC
PO Box 2110
Cupertino, CA 95015-2110

IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for news for technologists, managers and professors, the editorial objectives of IEEE **GRID** are to inform readers of newsworthy IEEE activities sponsored by local IEEE units (Chapters, Affinity Groups) taking place in and around the Bay Area; to publicize locally sponsored conferences and seminars; to publish paid advertising for conferences, workshops, symposia and classes coming to the Bay Area; and advertise services provided by local firms and entrepreneurs.

IEEE GRID is published as the **GRID** Online Edition residing at www.e-GRID.net, in a handy printable **GRID.pdf** edition at the end of each month, and also as the **e-GRID** sent by email twice each month to more than 24,000 Bay Area members and other professionals.

Editor: Paul Wesling
IEEE **GRID**
PO Box 2110
Cupertino CA 95015-2110
Tel: 408 331-0114 / 510 500-0106 /
415 367-7323

Fax: 408 904-6997
Email: editor@e-grid.net
www.e-GRID.net

From the editor . . .

As summer wanes and the kids get ready to go back to school, the pace of conferences picks up again. We are fortunate in the S.F. Bay Area – many conferences that "travel around" year to year will decide to come to SF, San Jose or Santa Clara every few years. You'll see some of them profiled on pages 4 through 12 in the **GRID.pdf**.

There are other opportunities to master new skills and get fresh insights – Chapter meetings are starting up again, with plenty of fresh topics. I know about a few of them (see table on Page 1), but more will certainly be added over the next few weeks. For a current snapshot of what's coming up, always refer to the GRID website at **www.e-grid.net** (and especially the QuickRef Calendar).

I hope you'll find something of interest in this issue of the **GRID** – perhaps a meeting you "just need to attend" or a Course that'll get you ready for a new assignment.

Paul Wesling, editor

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

Professional Services Marketplace – editor@e-GRID.net for information

Say you found them in our GRID MARKETPLACE

VOICE COIL MOTORS
Design - Control - Fabricate - Test
J. Arthur Wagner, Ph.D.
1649 Fair Orchard Ave.
San Jose, CA 95125
wagneretal@sbcglobal.net
(408) 269-7044 (408) 206-3049 cell

Valon Technology, LLC
valontechnology.com
stuart@valontechnology.com
RF and Wireless Product Design & Development
- System Engineering
- Test & Measurement
- Schematic Capture & PCB layout
- Expert Witness

Redwood City (650) 369-0575

ANSYS Channel Partner
- Multiphysics, Multidisciplinary Engng
- CFD, Stress, Heat Transfer, Fracture
- Fatigue, Creep, Electromagnetics
- Dynamics, Design Optimization
- Linear/Nonlinear Finite Element Analyses

Ozen Engineering (408) 732-4665
info@ozeninc.com www.ozeninc.com

MET Laboratories
EMC – Product Safety
US & Canada
- Electromagnetic Compatibility
- Environmental Simulation
- Design Consultations
- NEBS (Verizon ITL & FOC)
- Wireless, RFID (BQTF & EPCglobal Test Lab)
- Product Safety Cert.
- Full TCB Services
- MIL-STD testing
- Telecom

Facilities in Union City and Santa Clara
www.metlabs.com info@metlabs.com 510-489-6300

Device Thermal Characterization
Package Thermal Characterization
Thermal Test Boards
Thermal Test Equipment & Fixtures

Bernie Siegal
Thermal Engineering Associates, Inc.
650-961-5900
info@thermengr.com www.thermengr.com

Patent Agent
Jay Chesavage, PE
MSEE Stanford
3833 Middlefield Road, Palo Alto 94303
info@file-ee-patents.com
www.File-EE-Patents.com
TEL: 650-619-5270 FAX: 650-494-3835

IEEE-CNSV
Consultants' Network of Silicon Valley
Become a member
Find a Consultant
Submit a Project
CaliforniaConsultants.org

GRID.*pdf*
e-GRID

Do you provide a service?
Would you like more inquiries?

- Access 25,000 engineers and managers
- IEEE Members across the Bay Area
- Monthly and Annual Rates available

Visit our Marketplace (page 3)

Download Rates and Services information:
www.e-grid.net/docs/marketplace-flyer.pdf

FLASH: Fast, Rugged, Mobile, Low-Power, Small

Flash Memory Summit 2007

August 7-9, 2007 Santa Clara Marriott, Santa Clara

The Flash Memory Summit program is designed to provide attendees with practical information on the current state of flash memory and its applications.

Topical Areas

- Design methods
- Flash software
- Standards
- Flash Controllers
- Consumer applications
- Embedded applications
- Programming methods
- Hybrid systems (disk or DRAM)
- Interoperability
- Security/content protection
- Testing
- Flash disks
- Memory cards
- Other non-volatile technologies
- Computer applications
- Flash based µ-controllers

Advance Program now posted!

KeynoteTalks

"**Flash Vision**" by Eli Harari, SanDisk
"**The Evolving Role of Flash in Memory Subsystems**" by Ed Doller, Intel
"**SSDs: The Next Killer App in Flash**" by Jim Elliott, Samsung

Participating companies include: Intel, Samsung, SanDisk, Microsoft, Dell, Datalight, PNY, Kingston Memory, SST, STEC, Hagiwara, Smart Modular, Micron, Toshiba, Xiotech, Seagate and many more!

Exhibitor Information: Alan Land, 760-212-5718.

- Learn how to make your products rugged, low-power, fast & small
- Find out about new flash software, controllers and formats such as SD cards & USB drives
- Hear about the latest market trends and much more!

Half-Day Tutorials

- Introduction to Flash Memory
- Designing Flash-Based Products
- Flash in the PC: New Approaches to Higher Performance
- Flash on the Go: Designing for Mobile Apps
- What Can We Learn from the iPod Revolution?

…Plus Venture Capital Presentations

Roundtable:

"**What is the Next Killer App for Flash?**"

Registration now open.

Visit the Flash Memory Summit website:

www.flashmemorysummit.com

IEEE Professional Skills Courses

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Managing Across Cultures

- Date/Time: Tuesday, Aug 7, 8:30AM – 4:30PM
- Location: Trimble Navigation, Sunnyvale
  Fee: $375 for IEEE Members; $450 non-members

Presentation Skills

- Date/Time: Thursday, Aug 9, 9:00AM – 5:00PM
- Location: Cypress Semiconductor, San Jose
- Fee: $450 for IEEE Members; $525 non-members

High-Impact Communication

- Date/Time: Tuesday, Aug 21, 8:30AM – 4:30PM
- Location: Tibco, Palo Alto
  Fee: $375 for IEEE Members; $450 non-members

Creative Problem Solving

- Date/Time: Wednesday, Aug 15, 8:30AM – 4:30PM
- Location: Sybase Inc, Dublin
- Fee: $375 for IEEE Members; $450 non-members

Coaching Others to Excellence

- Date/Time: Wednesday, Sept 12, 8:30AM – 4:30PM
- Location: Dionex Corporation, Sunnyvale
  Fee: $350 for IEEE Members; $425 non-members

Interviewing and Hiring the Best Talent

- Date/Time: Thursday, Oct 18, 8:30AM – 4:30PM
- Location: Tibco, Palo Alto
  Fee: $375 for IEEE Members; $425 non-members

Improve your skills – register for one of these classes, or for others coming up this summer. Bring a team!

For complete course information, schedule, and registration form, see our website:

www.EffectiveTraining.com

ROBO DEVELOPMENT
CONFERENCE AND EXPO 2007

October 25-26, 2007

San Jose McEnery Convention Center

The International Technical Design and Development Event for the Personal, Service and Mobile Robotics Industry

RoboDevelopment is a multifaceted educational forum and trade show dedicated to addressing the technical issues involved with the design and development of commercial robotic products. The exposition hall provides attendees with hands-on access to the latest design and development solutions for producing mobile robotics and intelligent systems technology, while the keynotes and general sessions are specifically designed to impart to technical professionals the information they need to develop the next generation of personal, service and mobile robots.

TECHNICAL TRACKS

- Design, Development and Standards
- Tools and Platforms
- Enabling Technology

KEYNOTE SPEAKERS

Tandy Trower, Prgm Manager, Microsoft Robotics Group
Paolo Pirjanian, President and CEO, Evolution Robotics
Lloyd Spencer, CEO, Coroware
Dan Kara, President, Robotics Trends

TOPICS COVERED IN THE SESSIONS

●·The Robotics Engineering Design Process ●·Robot Types and Form Factors ●·Localization, Navigation and Mapping ●·Robotic Control Architectures ●·Hardware and Software Architectures for Robotic Systems ●·Machine Learning ●·Data Acquisition and Sensor Fusion ●·CAD/CAM Tools For Robotics Development ●·Software Development Kits and Modeling Tools ●·Operating Systems: Linux, Windows, MTOS, VxWorks, QNX, Others ●·Robotics Kits and Component Suppliers ●·Drive Trains - DC Motors, Servo Motors and Stepper Motors ●·Locomotion - Wheeled, Tracked and Legged Systems ●·Batteries and Power Systems ●·Manipulators and End Effectors … and more

Earlybird Rates thru September 14 – save $200

More information, and to register:

www.robodevelopment.com

Contact us for exhibiting information:
Dan Kara, dk@roboticstrends.com, 508-663-1500 x329

Opportunities for Volunteers: Engineers Needed for K-12 Programs

We need engineers/developers who can assist with programs from Kindergarten through 12th grade, in our local public schools. Give us a hand ….

For Fall/Winter 2007

- Future City
- Lego Robotics : Middle schools
- Book Sorting

For Spring 2008

- Engineer's Week
- Science Fair
- Robotics: High schools
- Career Fair: High schools

We'd appreciate your help.
Contact : David Fong **dfong@ieee.org**

Visit our SCV K-12 Website, to see what we're doing and how you can help:

www.ewh.ieee.org/r6/scv/k-12

Reduce your taxes by donating stocks or cash to support Santa Clara Valley K12 activities! Send to:
IEEE Foundation, Incorporated
IEEE Development Office
c/o Santa Clara Valley K-12 Education Fund
445 Hoes Lane
PO Box 1331
Piscataway, NJ 08855-1331

Support Santa Clara Valley K12 funding activities by signing up for eScrip at www.escrip.com

using our group id: (IEEE Santa Clara Valley Section K12, or Group ID# 500002476)
…and register your credit cards (VISA, Macy's VISA) so that your purchases using your cards at places like Macy's, Cosentino's, Draeger's, PW Supermarkets, Whole Foods, Big 5, PepBoys, Big O Tires, OfficeMax, Carl's Jr, LeBoulanger … will be credited towards our group.

Any questions, contact David Fong **dfong@ieee.org**

Nara Institute of Science and Technology (NAIST) presents a One-Day Seminar in the Santa Clara Valley:

IT and Materials Technologies: Bio Nano Process, Sound Separation, Solar-Cell Inspection and Other Technologies from Japan

Tuesday August 21, 2007
9:30 AM – 5:00 PM

Place: UCSC Extension, Moffett Business Park, 1180 Bordeaux Drive, Sunnyvale

Morning Topics: (9:30 AM – Noon)

Development and Properties of Luminescent Chalcogenide Nanocrystals

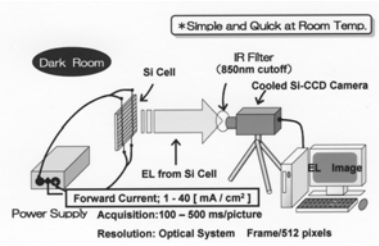
Professor T. Kawai

Emissive CdTe nanocrystals Quantum Efficiency>90%

CdTe nanocrystals showing high emission quantum yield with no protecting layer – act as efficient emitting and photo-sensitive material in photo-polymerization system. Potential as efficient high-density optical recording medium and solar cell.

A Versatile Tool for the Diagnosis of Crystalline-Silicon Solar Cells Using Electroluminescence

Professor T. Fuyuki



Forward bias electro-luminescence intensity is related to minority carriers. Defects, grain boundaries, cracks are detected as dark spots, lines, and areas. Versatile tool to evaluate cell fabrication process and performance.

Lunch is served at Noon

Registration: **BEFORE AUGUST 7** There is **no charge** for this seminar, but we need an accurate count by August 7 in order to properly schedule conference room space.

Register today, to assure a seat. Fax/mail/email to:
UCSC Extension: NAIST Seminar
1101 Pacific Avenue, Suite 208
Santa Cruz, CA 95060 FAX: +1-831-427-1827
Email: ltran@ucsc-extension.edu

Name(s):

Company:

Addr:

City/ZIP: Phone:

Email:

We will confirm by email. (please print clearly)

After August 7, call for availability: Lena Tran, 408-861-3854

Afternoon Topics: (1:00 PM – 5:00 PM)

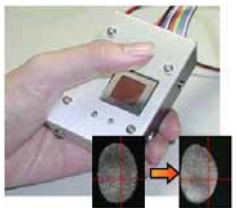
Pocket-Size Real-Time Blind Source Separation (BSS) Module for Hands-Free Speech Acquisition

Associate Professor H. Saruwatari

BSS estimates original sound sources using mixed signals detected by multiple microphones. This algorithm uses independent component analysis and binary masking, imitating human brain and ears. Potential for clear reception of cell-phone call amid noise. Portable, with a delay time of less than 50msec.

Tactile Sensors for Advanced Robotics

Assistant Professor J. Ueda



Vision-based tactile sensor and slip prediction method; Fingerprint pointing device for mobile application; Teaching playback of dextrous robot manip-ulation; MRI compatible force sensor. Tactile information processing for robotic manipulation and human-machine interfaces

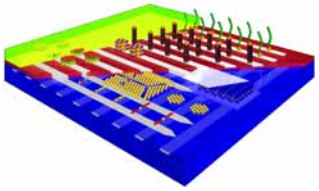
CMOS Technologies for Biological and Medical Applications

Professor J. Ohta

Highly functional/versatile biomedical devices: retinal prosthesis, brain implantation, and future issues for bionic human uses of implantable CMOS technologies.

Bio Nano Process – Fabrication of Inorganic Nanostructures by Protein Supramolecules

Professors I. Yamashita and T. Fuyuki



Self-organization and biomineralization of bio-supramolecules for fabricating inorganic structures for nano-electronic devices. Memory nanodot array in a floating gate memory; a proposed biological path to nano-electronics.

Right after the seminar …

Come meet the staff from Japan's NAIST. Discuss their new technologies, and your own technologies and potential applications.

Details: **www.e-grid.net/conf/NAIST.html**

More about NAIST's Seminar: www.naist.jp/index_e.html

ISSM 2007

16th Annual International Symposium on Semiconductor Manufacturing

October 15 – 17, 2007
Marriott Hotel, Santa Clara

Technical. Informative. Advancing.

ISSM is the industry's largest assembly of semiconductor manufacturing professionals dedicated to driving technology innovation and operational excellence within the industry.

Industry leaders will share ideas and collaborate on new models for semiconductor manufacturing that redefine the value chain and demonstrate new levels of agility and efficiency in meeting the needs of their customers. The ISSM 2007 Conference features presentations and posters from leading device manufacturers, suppliers, and academia worldwide.

Program topics for this year's symposium include:

- Manufacturing Strategy & Operations Management
- Manufacturing Control & Execution
- Process & Material Optimization
- The Green Factory - The Role of Environment, Health, Safety
- Advanced Process & Metrology Equipment
- Supply Chain Integration
- Yield Enhancement & Contamination Control
- Design for Manufacturing
- Factory Design & Automated Material Handling
- Process & Equipment Control
- Advanced Packaging & Test

ISSM 2007: *Maximizing Operational Efficiencies at the Leading Edge*

Keynote Speakers:

- "One Touch" Supply Chain
  Susan Graham Johnston, VP, Sun Microsystems, Inc.
- Twelve Types of Innovation That Will Save Your Company
  Rich Karlgaard, Publisher of Forbes
- Optimizing Fab Performance
  Michael Splinter, CEO, Applied Materials
- Technology and the Equipment Industry
  Nick Bright, Executive VP, Lam Research Corporation
- Optimizing Memory Operations at the Leading Edge
  Mark Durcan, COO, Micron Technology, Inc.
- Challenges and Opportunities Facing the Semiconductor Industry
  Jackson Hu, Chairman and CEO, UMC Corporation
- Increasing the Role of Indirect Materials for Semiconductor Manufacturing
  Susumu Kohyama, President and CEO, Covalent Materials Corp
- Less is More
  Paul Westbrook, Sr. Technologist, Texas Instruments

Financial Panel:

- Financial Panel Discussion: Remaining Public? Or Going Private?
  Moderated by Mihir Parikh and Frank Quattrone, Aquest Systems
  Panelists from Morgan Stanley, The Blackstone Group, Bear Stearnes

Register. Early bird discounts for both IEEE members and non- members thru Sept. 17. **Visit** the ISSM website at

www.ISSM.com

Reach your target audience. For sponsorship opportunities visit: **www.issm.com/sponsorship.htm**

Santa Clara University School of Engineering Graduate Programs

SCU Summer Open University

Have you ever wanted to continue your education in engineering while you continued working? Santa Clara University's School of Engineering offers graduate degree and non-degree programs to both full-time students and working professionals. Simplified registration for the Summer Open University. Graduate-level instruction. Up to 12 units may be transferred to a graduate-degree program.

Prepare for that next project or assignment!

Register by July 27

Classes July 30 – Aug 31

Santa Clara University

Evening classes:

- Linear Algebra I and II - Database Systems - XML Technologies and J2EE - Scripting with Python
- Semiconductor Device Technology Reliability
- Effective Written Technical Communication
- Global Software Management (Advanced)
- Web Services *(and more)*

Early-morning class:

- Electronic Circuits

Email Wan Chen with inquiries: **WQChen@scu.edu**

Located in the heart of Silicon Valley, with easy parking.

Choice of classes in Session III:

- Session III - 5-week classes (**July 30 - August 31**)
  … plus a number of one-day Saturday classes

To learn more, sign up for a Wednesday early-evening information session on **Aug 8 or 29**: Visit

www.scu.edu/engineering/graduate/rsvp.cfm

Review summer Open University courses:

www.scu.edu/ieee2

CICC IEEE Custom Integrated Circuits Conference

Showcase for circuit design in the heart of Silicon Valley

September 16-19, 2007
DoubleTree Hotel – San Jose

What are the latest trends and innovative circuit techniques for analog and digital ICs? How are circuit designers solving the major issues of power, variation, noise, jitter, GHz performance, system-on chip integration, and limits to scaling? The CICC technical program features new, state-of-the-art developments -- over 160 papers plus posters and exhibits in a broad range of circuits, applications, tools, and design techniques.

Technical Program Highlights

• Future Microprocessor Interfaces • A sub-2.5V, 100-Gb/s Serial Transceiver • A 0.25um 0.92mW per Mb/s Viterbi Decoder for Ultra-Low-Power WLAN Communication • A high performance MIMO/diversity direct conversion transceiver IC for WiMAX • A 65uW, 1.9 GHz RF to Digital Baseband Wakeup Receiver for Wireless Sensor Networks • A Single-Chip UHF RFID Reader in 0.18 um CMOS … *and much more*

Keynote and Luncheon talks

"**The Wireless Revolution Continues: Can Technology Keep Up with the Challenge?**" Bill Krenik, TI

"**Growing up with Batteries and Wires**," Paul Brokaw, Fellow - Analog Devices, of "Brokaw Road" and "Brokaw Bandgap"

Education Sessions on September 16

A valuable opportunity to refresh key skills in traditional circuit-design methods and acquire knowledge in vital new areas.

Track 1: High Speed Serial I/O Design Techniques

- Introduction to High-Speed I/O
- Clocking and CDRs
- Introduction to Signal Integrity
- Jitter Analysis
- Circuit & System Aspects of I/O Equalization

Track 2: Mixed Signal SOC Design Methodology

- Analog Verification
- Top-Down Design Methodology
- Top-Down Design of RF Transceivers using VHDL
- Top-down Design of Digital Circuits

Track 3: Low Power Embedded ADC Design

- System Aspects
- Pipeline ADC Design
- Sigma Delta ADC
- Case Study

Registration now open; best rates through **August 24**.

For full information and registration details:

www.ieee-cicc.org

Sponsored by the Solid State Circuits and Electron Devices Societies

Co-Sponsor: **Santa Clara Valley Section, IEEE**

SILICON VALLEY TECHNICAL INSTITUTE

Summer Courses with labs

Design of Radio Frequency Integrated Circuits

12 week course, T/TH 6:00PM-9:00PM (Starts: **July 10**)
A balance of communications, physics and IC design. Includes high-speed amplifiers, LNA, Mixer, VCO, PA, PLL and other RF blocks.

MATLAB & Simulink for Design & Digital Signal Processing

12 week course, M/W 6:00PM-9:00PM (Starts **Aug 20**)
Hands-on, from basic concepts in discrete time systems, filter design and implementation all the way to advanced concepts of multi-rate systems; balanced mix of theory and practice.

Analog CMOS Integrated Circuit Design

12 week course, T/Th 2:00PM-5:00PM (Starts **Aug 20**)
A detailed review of the principles, concepts, and design methods used for current state-of-the-art analog circuits; common analog building blocks; more complex analog circuits. HSPICE simulations are used extensively to augment the text/lecture material.

Discount of $40 for IEEE Members on 12-week courses.

Upcoming 1- and 2-day Seminars:

Aug 3: **Micro-Electro-Mechanical Systems (MEMS) - Technologies and Opportunities**

Aug 3: **Design-for-Yield & Design-for-Manufacturing (DFY/DFM) - Principles and Challenges**

Aug 10: **Fuel Cell Technology & Manufacturing toward Clean-Energy Applications**

Aug 15: **Signal Integrity (SI) and Noise Issues in Nanometer VLSI/SoC Designs**

Sept 7: **Solar Energy Technologies, Trends and Business Opportunities**

Discount of $30 for IEEE Members on Seminars.

Get more information:

www.svtii.com/SVTI-calendar.htm

Review all SVTI offerings: **www.svti.org**

FSA Suppliers eXpo & CONFERENCE

September 12, 2007 | Santa Clara, California USA | Santa Clara Convention Center

The FSA **Suppliers Expo & Conference** is the industry's must-attend exposition and conference. Featuring over 100 exhibiting companies and a full day of educational programming, this event strives to provide you with the opportunity to meet with potential partners and hear from industry experts regarding the topics most relevant to today's semiconductor industry.

Program:

FSA Annual Briefing: Jodi Shelton, Executive Director, FSA
Panel: Consumer to OEM to Semiconductor: How Innovation Drives the Semiconductor Supply Chain
Keynote: Rick Cassidy, President of TSMC North America
Panel: Successful Collaboration in an Outsourced Industry

Exhibits: Open 9:00 AM – 6:00 PM

Organized by **FSA** (Fabless Semiconductor Association)

GOLD SPONSORS ARM Chartered UMC FAB tsmc SILVER SPONSOR WIPRO

As supply chain and original equipment manufacturer costs increase, the chip designer's ability to stay innovative and profitable in today's semiconductor industry remains a challenge. The FSA Suppliers Expo addresses this growing industry concern. The goal: to provide you with knowledge you need to keep your business competitive in today's marketplace.

FREE ATTENDEE REGISTRATION
When you register by September 7, 2007

Onsite registration is $25
Complimentary Parking

For full information, listing of exhibitors and registration details, please visit:

fsa.org/suppliers_expo/usa2007/ieee

Co-Produced by the MIT/Stanford/UC-Berkeley Nanotechnology Forum

Energy Nanotechnology International Conference

ASME SETTING THE STANDARD

September 5-7, 2007 Santa Clara University

The 2nd Energy Nanotechnology International Conference will focus on state-of-the-art research and development in energy-related materials, nanoscale phenomena, devices, systems, manufacturing, and commercialization. The connection between nanotechnology and energy is inextricable – many unique physical phenomena occur at the nanoscale through confinement of allowable states of basic energy carriers (electrons, phonons, and photons). The consequences of these phenomena are manifested in various areas of energy science and engineering and are being exploited with every-improving efficacy to improve energy technologies.

Solar: fundamentals, solar-thermal, high-efficiency devices, low-cost devices
Biofuels and Carbon-Neutral Technologies: biodiesel, ethanol production, raw materials
Direct Thermal Energy Conversion and Harvesting: thermoelectrics, nanoscale transport, carrier coupling
Electrochemical Conversion and Storage: fuel cells, batteries, membranes, electrodes, systems
Hydrogen: production, storage, utilization
Fossil fuels: coal gasification, reforming, co-generation, carbon sequestration
Materials/Manufacturing: nanomaterials, scale-up, heterogeneous integration
Commercialization: leading Venture Capitalists will evaluate new product ideas in all renewable energy areas and will provide feedback on steps needed for successful commercialization

ASME 5th Nano Training Bootcamp

Detailed and tutorial-based; given by experts in academia and industry; providing intense sessions on fundamentals, fabrication, characterization & materials, and devices; at Santa Clara Univ.

www.asmeconferences.org/nanobootcamp07

Earlybird rates through July 30 – save $50

asmeconferences.org/EnergyNano07

Flash Memory SUMMIT

2nd Annual Flash Memory Summit
August 7-9, 2007
Santa Clara Marriott
Santa Clara, CA

Learn how to make your products
Rugged, Low-Power, Fast and Small
at the only conference dedicated to flash memory!

Attend this year's Flash Memory Summit for the latest practical information on flash memory and the most recent developments in flash memory applications. The Summit consists of half-day tutorials, panel discussions, keynotes, presentation sessions, workshops, special sessions and exhibits.

Topics of Interest

- Design methods, best practices, emerging standards
- Consumer application requirements
- Flash software, controllers, and formats such as SD cards and USB drives
- Embedded applications
- Hybrid flash and HDD storage
- Storage security and programming requirements
- SDDs in computers, computer applications and flash-based microcontrollers

> "NAND flash has emerged as king of the memory jungle and now drives the memory process road map, a domain traditionally held by the DRAM."
> – Malcolm Penn, Future Horizons

Participating Companies include Intel, Samsung, SanDisk, Datalight, Dell, PNY, Kingston Memory, SST, STEC, Hagiwara, Smart Modular, Micron, Toshiba, Xiotech, Seagate and many more.

Sponsorship and Exhibiting Information:
Alan Land +1-760-212-5781
alan@flashmemorysummit.com

Who Should Attend?

- Designers of hardware, software, consumer electronics, memory and embedded systems
- Applications, storage, communications, computer,
- systems, and test engineers
- Storage specialists
- Engineering managers, systems analysts, solution providers and consultants
- VARs, OEMs, system integrators, venture capitalists, marketing and product managers

Keynote Speakers

- Ed Doller, IBM
- Jim Elliott, Samsung
- Eli Harari, SanDisk

Free Special Market Research Session on State of the Flash Memory Market (included with complimentary exhibits & open sessions registration)

For more information, and to register online:

flashmemorysummit.com

ITC, the cornerstone of TestWeek™, is the world's premier conference dedicated to the electronic test of devices, boards and systems-covering the complete cycle from design verification, test, diagnosis, failure analysis and back to process and design improvement. At ITC, test and design professionals can confront the challenges the industry faces, and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers.

With the theme "Facing Nanometer-Technology Test Challenges," the 2007 conference will focus on breakthrough ideas to address the challenges of providing high-quality, cost-effective tests for nanometer-technology designs.

Keynote and Invited Addresses

Managing Test, Yield, Quality, and Cost in the Fabless Manufacturing Model, *Chris Malachowsky, NVIDIA Fellow and Senior Vice President*

The Impact of Globalization on Test and the Test Engineer, *Greg Jordan, Sr. Director, Manufacturing Test Engineering, Cisco Systems, Inc.*

On the Need for Convergence Between Design Validation, *Siva Yerramilli, General Manager, Design and Technology Solutions Manufacturing Group, Intel Corporation*

It's Not What You Can Make – It's What You Can Test, *Robert Daasch, Professor, Electrical and Computer Engineering, Portland State University*

Welcome Reception

Tuesday, Oct. 23, 6:15 - 8:00 PM, Hyatt Regency Hotel

World-Class Exhibits

Tuesday 10:30 AM – 4:00 PM
Wednesday 9:30 AM – 5:30 PM
Thursday 9:30 AM – 2:00 PM

Free exhibits-only admission on Wednesday afternoon and all day Thursday.

Free Parking at the Santa Clara Convention Center

IEEE

IEEE COMPUTER SOCIETY

Sunday Full-day Tutorials

DFX: The Convergence of Yield, Manufacturing, and Test
Delay Testing: Theory and Practice
Statistical Screening Methods Targeting "Zero Defect" IC Quality and Reliability
Dealing with Timing Issues for Sub-100-nm Designs – from Modeling to Mass Production
Practices in Analog, Mixed-Signal and RF Testing
Test Strategies for System-in-Package
Memory Test Challenges – A Practical and Implementation View of BIST and Other DFT Techniques
Digital Timing Measurements – From Scopes and Probes to Timing and Jitter

Monday Full-day Tutorials

IEEE 1500 – Building a Compliant Wrapper
Delay Test: A Practical Approach
Advanced Memory Testing
Scan Compression Techniques: Theory and Practice
Wafer Probe Test Technology
Design-for-Manufacturability
Understanding Failure Mechanisms and Test Methods in Nanometer Technologies
Design-for-Testability for RF Circuits and Systems

33 Technical Sessions

● Microprocessor Test ● Improving Test Quality ● Memory Testing ● New SERDES Test Techniques ● Getting Accustomed to Unknowns ● SOC Test ● Advanced Diagnosis Algorithms ● Breaking the 10-Gb/s Barrier ● Advances in ATPG and Delay Test ● HF in Volume Production ● Advanced Characterization Methods ● Power-aware Testing ● New Advances in Detecting PCBA ● Structural Defects ● Towards More Efficient Defect Diagnosis ● New Tests for PLLs ● Test and Debug Data Reduction ● Advances in DFT ● Functional and Outlier Test ● Characterization with Delay Test, IDDQ and Probing ● The New ATE: Protocol-aware ● Fault Simulation ● RF Test Methods ● Fault and Error Tolerance in Nanotechnologies ● System Issues with Test ● Defect Tolerance in Microprocessors … *and more*

Friday All-day Workshops

● Design-for-Manufacturability and Yield ● Current- and Defect-based Testing ● Automated Test Equipment Vision 2020

Discount Rates – Register by **September 24**
Download the full Advance Program today:

www.itctestweek.org

Exhibit at ITC!

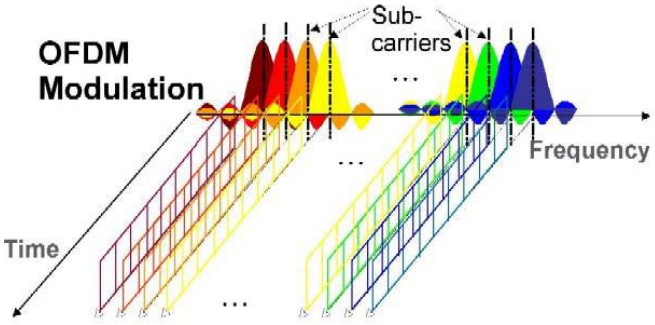
Contact Jim Monzel, IBM, **jmonzel@us.ibm.com**

SCV Chapter, IEEE Communications Society *SCU Institute for Communications Circuit Design*

OFDM Workshop

Monday October 8, 2007
Santa Clara University, Santa Clara

Orthogonal Frequency-Division Multiplexing (**OFDM**) implementation and Cross-layer Optimization have become topics of intense research interest in companies and universities around the world. Come to the **OFDM Workshop** at Santa Clara University to share your ideas in these areas or just to catch up. This year's workshop contains eight outstanding industrial and academic speakers.



Speakers

- **John Cioffi**, Stanford University
- **Babak Daneshrad**, UCLA
- **Alan Gatherer**, Texas Instruments
- **George Ginis**, ASSIA
- **Mike Fitz**, Northrup Grumman
- **Ayman Naguib**, QualComm
- **Milica Stojanovich**, MIT
- **Lee Swindlehurst**, ArrayComm
- **Steve Weinstein**, Consultant

Plenty of free parking; lunch/reception provided.

$100 if registered by **Sept. 5** ($90 for IEEE members)

To get **full information** and the registration packet, please visit our website:

iccd.engr.scu.edu

IEEE SCV-CAS TUTORIAL

Broadband and RF Circuit Analysis and Design in CMOS Technology Part II

Saturday Sept 15, 2007 – 8:30 AM – 1:00 PM

at Cadence Design Systems – Bldg 5
2655 Seely Ave, San Jose

This tutorial, a continuation of the **Sept 2006** event, will familiarize engineering professionals with both classic and innovative new broadbanding techniques for CMOS technology amplifiers appropriate for state-of-the-art communication system applications, with a focus on **Distributed Amplifiers**. A unified circuit broadbanding strategy is discussed, as is a practical methodology for the monolithic realization of narrowband radio-frequency (RF) amplifiers. Because broadband and RF design necessarily entails the incorporation of suitable matching filters in signal flow paths, a reasonably extensive discussion of lossless filter architectures is incorporated in the tutorial. All theoretic and conceptual disclosures are verified through the results of realistic SPICE simulations.

Instructor: **Dr. John Choma**, Fellow, Scintera Networks, and Professor of EE & Systems Architecture Engineering, Univ of Southern California

Registration: 8:30 – 9:00 AM (includes pastries/coffee)
Sponsored lunch: 12:15 – 1:00 PM

Tutorial Outline:
9:00: "Introduction and Overview" by Dr. William Kao
9:15: "Tutorial Part III" by Dr. John Choma
10:45: "Tutorial Part IV" by Dr. John Choma

Topics: Overview of MOS Transistor Modeling; Noise Sources In NMOS and PMOS Devices; Gain and Bandwidth Optimization in Common Source Amplifiers; Broadband Architectures; Lossless Filters; Linearity Considerations

A CD of all lecture material and related notes will be provided to all attendees.

Registration Fee:
IEEE Member $40 Non-Member $50

Registration Deadline August 31 (postmarked by Aug 31)
After Augsut 31 – if Space Available, $5.00 Surcharge

See full Tutorial Description for prerequisites and other details:

www.ewh.ieee.org/r6/scv/cas

SCV Lasers and Electro Optics

TUESDAY August 7

Low-Cost Solar Cells Exploiting Silicon Ink Technology

Speaker:	Homer Antoniadis, PhD, Chief Technology Officer, Innovalight
Time:	Pizza and drinks at 7:00 PM; Presentation at 8:00 PM
Cost:	donation for refreshments
Place:	National Semiconductor Building E Conference Center, Santa Clara
RSVP:	by email to ieeescvleos-rsvp2007@yahoo.com
Web:	www.ewh.ieee.org/r6/scv/leos

We will present a novel concept for low cost solar energy production using silicon nanotechnology. With a mix of nanotechnology, proven silicon reliability, and ink formulations, the company is developing a low-cost manufacturing platform to reduce the cost of producing electricity compared to current technologies. We will examine the promise of taking current polysilicon-based solar cells (90 percent of market today) to a completely new level of cost. The high cost of production of solar cells today (even with heavy subsidies) has been one of the major factors inhibiting the overall growth of solar energy as a market. Our silicon nanocrystalline ink holds the promise to bring the cost of solar panels to an order of magnitude lower than today's polysilicon technology.

Homer Antoniadis, PhD, is the Chief Technology Officer at Innovalight, Inc., a venture-funded technology startup developing disrupting solar power generating products based on nanosized silicon. Prior to Innovalight, Homer was the Head of OLED product development at OSRAM Opto Semiconductors Inc. and the Program Director for developing organic light emitting sources. He held positions at Xerox Corporation and as a principal research engineer/member of the OLED team at Hewlett-Packard Labs. He is widely recognized as a regular invited lecturer and conference chair at leading industry events. Homer has more than 50 publications in photovoltaics, OLEDs, polymer materials and amorphous silicon and has 17 issued US patents. Homer has a PhD and MS in Physics from Syracuse University and a BS in Physics from Ioannina University, Greece.

SCV Electron Devices

TUESDAY August 14

Unlocking the Potential of Solar Photovoltaics

Speaker: Charlie Gay, VP & GM, Solar Business, Applied Materials
Time: Social at 6:00 PM; Presentation at 6:15 PM
Cost: none
Place: National Semiconductor Corp. Building E-1 - Auditorium CMA, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds

In the next 60 minutes the sun will hit the earth with enough energy to meet all of the world's power needs for one year ... if only we could harness it. Solar photovoltaics (PV) is a simple solution to a huge problem facing the world, and we have reached a tipping point that puts solar in true reach. This talk will address the state-of-the-art in conversion of sunlight to electricity, the companies and countries making a meaningful impact on advancing the introduction of PV, and an overview of ways that individuals and governments should act today to help accelerate solar and put the power, quite literally, into the hands of the people.

Charlie Gay was named corporate vice president and general manager of the Solar Business Group at Applied Materials in 2006. An industry veteran with over 30 years of experience in the solar industry, Dr. Gay is responsible for establishing and building Applied Materials' solar business.

Dr. Gay is also a co-founder of the Greenstar Foundation, an organization that delivers solar power and internet access for health, education and microenterprise projects to small villages in the developing world. Greenstar has been recognized for its innovation by the World Bank, the Stockholm Challenge, the Technology Empowerment Network and the Tech Museum Awards.

Dr. Gay began his career in 1975 designing solar power system components for communications satellites at Spectrolab, Inc. and later joined ARCO Solar, where he established the research and development program and led the commercialization of single crystal silicon and thin film technologies. In 1990, Dr. Gay became president and chief operating officer of Siemens Solar Industries and from 1994 to 1997, he served as Director of the U.S. Department of Energy's National Renewable Energy Laboratory, the world's leading laboratory for energy efficiency and renewable energy research and technology. In 1997, Dr. Gay served as president and chief executive officer of ASE Americas, Inc., and in 2001 became chairman of the advisory board at SunPower Corporation.

Dr. Gay has a doctorate degree in physical chemistry from the University of California, Riverside. He holds numerous patents for solar cell and module construction and is the recipient of the Gold Medal for Achievement from the World Renewable Energy Congress.

SCV Solid State Circuits

THURSDAY August 16

A Digitally Modulated Polar CMOS PA with 20MHz Signal BW

Speaker: Amirpouya Kavousian, Stanford University
Time: Food and drinks at 6:00 PM; Presentation at 6:30 PM
Cost: Donation requested to partially cover food cost
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Dr., Santa Clara
RSVP: by email through ssc_scv_rsvp@yahoogroups.com
Web: www.ewh.ieee.org/r6/scv/ssc

Amirpouya Kavousian was born in Tehran, Iran in 1979. He received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran in 2001 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 2003, where he is working toward the Ph.D. degree in electrical engineering. His doctoral research focuses on the design of CMOS RF power amplifiers. He recently joined Quantenna Communications, Sunnyvale, CA as a design engineer.

The advent of high-bandwidth, highly spectral-efficient communication systems, such as IEEE 802.11g, has imposed tremendous challenges on power amplifier design. Since power amplifiers are often the most power-consuming block in a wireless system, their efficiency can have a determining impact on the battery lifetime of a system. However, the high linearity required of current and emerging wireless systems has typically mandated the use of highly linear low-efficiency traditional class-A designs. This talk presents a CMOS RF power amplifier that employs a digital polar architecture to improve the overall power efficiency while providing the linearity required of IEEE 802.11g systems. An experimental prototype of the polar power m CMOS technology, occupies a total dieμamplifier, integrated in am area of 0.18 x 1.8 mm^2, operates at 1.6GHz and achieves 6.7% PAE with -26.8dB EVM while delivering 13.6dBm linear output power

SCV Nanotechnology

TUESDAY August 21

Today's Scanning Probe Microscopy (SPM) in Nanotechnology: An Introduction

Speaker: Allen Gu, Applications Scientist, Pacific Nanotechnology Inc.
Time: Light lunch at 11:30 AM; Presentation at Noon
Cost: $5 for Members/Students, $10 for non-members
Place: SEMI World Headquarters, 3081 Zanker Rd., San Jose
RSVP: see website
Web: www.ieee.org/nano

Allen Gu is Scanning Probe Microscopy Scientist at Pacific Nanotechnology Inc in Santa Clara, an industrial leader in SPM business. He has 15 years' experience in nanotechnology-related research and development, including 7 years' expertise in AFM applications. He conducts the majority of the applications and research work at PNI. Prior to PNI, he worked on nano-material synthesis and nano device fabrication at the Institute for Micromanufacturing, Louisiana Tech University, where he was a Fellow Researcher focused on projects for the NSF, Air Force, and DOE. Previously, he contributed to key national chemical projects for the Chinese government with a combined value of $200M. He has authored numerous scientific journal publications.

He holds a Ph.D. in Nanosystems Engineering from Louisiana Tech University and a B.S. in Chemical Engineering from Nanjing University, China.

Scanning Probe Microscope (SPM) has been a mainstream characterization tool in nanoscience and nanotechnology since it was invented in 1986. The unique combination of 3D atomic resolution, easy operation and less sample selectivity makes it more attractive than other conventional microscopes. Recently, a number of advanced applications beyond visualizing structures have been developed in response to the research demand in property and functionality study of nanoscale materials and devices. It is achieved by utilizing specific interaction forces between specimen atoms and a sharp probe. Electrical properties, thermal conductivity, mechanical force and chemical information can be revealed at the same time as image acquisition. Although machine vendors are facing more challenges in design of a more reliable and faster scan mechanism, SPM is widely recognized as a powerful and affordable tool for seeing and measuring objects in this small format.

SCV Consumer Electronics

TUESDAY August 28

WirelessHD: High Bandwidth for Home Entertainment

Speaker: John Marshall, President, Wireless High Definition (WirelessHD) Consortium
Time: Pizza and drinks at 6:30 PM; Presentation at 7:00 PM
Cost: $5 for members, $10 for non-members
Place: Oak room at HP, 19447 Pruneridge Avenue (Building 48), Cupertino
RSVP: not required
Web: ewh.ieee.org/r6/scv/ce

John Marshall is President of the Wireless High Definition (WirelessHD) Consortium and President of WirelessHD, LLC, an organization comprising the world's leading consumer electronics companies, including LGE, NEC, Panasonic, Sony, Samsung, Toshiba. The Group is revolutionizing the home entertainment experience by enabling wireless, uncompressed sharing of high definition content among a wide range of home entertainment components (HDTVs, DVD players, et al.) and HD imaging devices (digital video and still cameras, et al.).

Marshall is also Vice President of Marketing for SiBEAM, Inc. Bringing ten years leadership of startup and Fortune 500 business operations, Marshall is responsible for SiBEAM's product and market vision and manages marketing, business development and sales. Since SiBEAM's inception, Marshall also led the formation of the WirelessHD™ special interest group focusing on A/V networking and currently serves as the president of WirelessHD, LLC.

Prior to joining SiBEAM, Marshall served as vice president of marketing and business development at 2Wire, Inc., a leading broadband services platform developer, supporting its growth from first product to market leadership on over $150M in worldwide revenue. Prior to 2Wire, Marshall co-founded 3Com's Wireless & Home Networking Division, capturing market leadership for its first product line in its first year. At 3Com prior, Marshall led emerging market development in ICE markets (information, communications, entertainment) from $40M to $400M revenue.

Prior to 3Com, Marshall worked for a marketing consultancy advising technology companies on market entry strategy, segmentation, pricing, and competitive analysis. In addition to his work at SiBEAM, Marshall has served on the advisory board of Ruckus Wireless, as president of the Home Phoneline Networking Alliance (HomePNA), the board of USC's Entertainment Technology Center (ETC) and the Association for Interactive Media (AIM).

Marshall holds a B.A. from Northwestern University and MBA from the University of Michigan's Ross School of Business.

SCV Electron Devices

THURSDAY September 13

Nanotechnology, Molecules and the Future of Electronics

Speaker:	Duncan Stewart, HP Labs
Time:	Social at 6:00 PM; Presentation at 6:15 PM
Cost:	none
Place:	National Semiconductor Corp. Building E-1 - Auditorium CMA, 2900 Semiconductor Drive, Santa Clara
RSVP:	not required
Web:	www.ewh.ieee.org/r6/scv/eds

"Nanotechnology" will solve every materials, electronics and biology problem we have, according to some of the latest techno-hype. Or destroy the world with self-replicating nano-robots, predicts popular fiction. We will take a look at what is real, what is not real, and what may never be real in this exciting field of nanoscale control over atoms and molecules. Particular emphasis will be given to nanoscale electronics, where Hewlett-Packard Labs has a strong effort in nanoelectronic devices, architectures, and manufacturing.

Duncan Stewart is a research physicist at Hewlett-Packard Laboratories in the Quantum Science Research group. He received a B.A.Sc. in Engineering Physics from the University of Toronto in 1992 and a Ph.D. in Applied Physics from Stanford University in 1999, where he studied nanoscale electron transport. He joined HP Labs in 1999, and has since worked extensively on nanoscale hybrid organic/inorganic devices, with efforts in both basic science and applied nanotechnologies. Basic science efforts focus on the challenging physical and chemical characterization of nanoscale interfaces, particularly organic/inorganic structures. Nanotechnology contributions include molecular-scale electronic switching, demonstrations of electronically addressed nano-crossbar memory at world-record densities, and the first demonstrations of nano-crossbar logic circuits with transistor-like functionality. Stewart has published more than 20 reviewed scientific papers and authored more than 20 patents in the area of nanoscale electronics and materials.

SCV Communications, with Circuits & Systems, Signal Processing

MONDAY September 17

Transceiver Designs for Multicarrier Transmission

Speaker: Distinguished Lecturer Prof. Yuan-Pei Lin, Department of Electrical and Control Engineering, National Chiao-Tung University, Taiwan
Time: Presentation at 6:00 PM
Cost: none
Place: National Semiconductor, Building E, Conference Room, 2900 Semiconductor Dr, Santa Clara
RSVP: not required
Web: www.comsocscv.org

Prof. Yuan-Pei Lin (S'93-M'97). IEEE CAS Distinguished Lecturer, 2006~2007. She received the B.S. degree in control engineering from the National Chiao-Tung University, Taiwan, in 1992, and the M.S. degree and the Ph.D. degree, both in electrical engineering from California Institute of Technology, in 1993 and 1997, respectively. She joined the Department of Electrical and Control Engineering of National Chiao-Tung University, Taiwan, in 1997. Her research interests include digital signal processing, multirate filter banks, and signal processing for digital communication, particularly the area of multicarrier transmission. She is a senior member of IEEE. She was a recipient of 2004 Ta-You Wu Memorial Award for outstanding research. She is currently an associate editor for IEEE Transaction on Signal Processing, EURASIP Journal on Applied Signal Processing, and Multidimensional Systems and Signal Processing of Academic Press.

The multicarrier transceiver has found applications in a wide range of wired or wireless transmission channels. It is typically called DMT (discrete multitone) for wired DSL (digital subscriber loops) applications such as ADSL (asymmetric DSL) and VDSL (very high-speed DSL), and called OFDM (orthogonal frequency division multiplexing) for wireless LAN (local area network) and broadcasting applications such as digital audio broadcasting and digital video broadcasting. For wireless transmission, the channel profile is usually not available to the transmitter. The transmitter is typically channel independent and there is no bit/power allocation. Moreover having a channel independent transmitter is of vital importance for broadcasting applications, where there are many receivers with different transmission paths. In wired DSL applications, the channel does not vary rapidly. This allows the receiver to send channel profile back to the transmitter through a reverse channel. In this lecture, we consider optimal transceiver design for two cases: (i) channel profile available at the transmitter; (ii) channel profile not available at the transmitter. In the first case, the transmitter is channel independent and the channel dependent part of the transceiver should be only at the receiver. The optimal transceiver that minimizes bit error rate rate subject to the same transmission power will be designed. For the second case, bit and power allocation can be used to exploit the disparity among the subchannel noise variances. The optimal transceiver that minimizes transmission power subject to the same transmission bit rate and the same bit error rate will be derived. Substantial gain can be achieved using the optimal transceiver, especially for moderate number of subcarriers. The popularity of system-on-chip (SOC) integrated circuits has led to an unprecedented increase in test costs. This increase can be attributed to the difficulty of test access to embedded cores, as well as long test development and test application times. This talk will present test resource partitioning techniques that facilitate low-cost SOC test. Topics to be covered include the recent IEEE 1500 standard for testing core-based SOCs and techniques for modular testing of digital SOCs. Test planning methods that involve the use of wrappers and test access mechanisms will be discussed. Test scheduling techniques for the concurrent testing of embedded cores at the SOC level will also be presented. Together, these techniques offer SOC integrators with the necessary means to manage test complexity and reduce test costs.

SCV Magnetics

TUESDAY September 18

State-of-the-art Ferrite Materials for Fundamental Research, Nano-science, and High-Frequency Applications

Speaker:	Prof. Vince Harris, Northeastern University, Boston
Time:	Cookies and drinks at 7:30 PM; Presentation at 8:00 PM
Cost:	none
Place:	KOMAG, 1710 Automation Parkway, San Jose
RSVP:	not required
Web:	www.ewh.ieee.org/r6/scv/mag

Prof. Vincent G. Harris received the B.Sc., M.Sc., and Ph.D. (1990) degrees in engineering from Northeastern University. He has also received the M.Sc. degree in engineering management from the University of Maryland (1995), and the M.Sc. degree in executive technology management from the Wharton School at University of Pennsylvania (2003). He is presently the William Lincoln Smith Chair Professor in the Electrical and Computer Engineering Department at Northeastern University.

Dr. Harris was a member of the technical staff at the Naval Research Laboratory (1990-2003). During his time at NRL he served as the head of the Complex Materials Section and the head of the Materials Physics Branch. In 2001 he established and assumed the position of director of the NRL Synchrotron Radiation Consortium. In 2004 he established the Center for Microwave and Magnetic Materials and Integrated Circuits, and continues to serve as its first director . The mission of this center is to develop high frequency materials and device solutions for next-generation radar and wireless communication electronics.

His research interests include materials design and the study of processing, structure, and magnetism in a wide range of materials. He has pioneered the use of synchrotron radiation techniques to relate the short range chemical and structural properties of materials to magnetism. He has published more than 170 technical articles, including book chapters and review articles on the topical areas of nanotechnology, magnetism, and magnetic materials. In addition, he holds nine patents and patent applications, and has presented more than 150 papers at national and international meetings. Dr. Harris is a Fellow of the American Physical Society and Senior Member of the IEEE.

Ferrite materials have long played an important role in power conditioning, conversion, and generation across a wide spectrum of frequencies (up to 10 decades). They remain the preferred magnetic materials, having suitably low losses, for most applications above 1 MHz, and are the only viable materials for nonreciprocal magnetic microwave and millimeter wave devices (including tunable filters, isolators, phase shifters, and circulators). Recently, novel processing techniques have lead to a resurgence of research interest in the design and processing of ferrite materials as nanoparticles, films, single crystals, and metamaterials. These latest developments have set the stage for their use in emerging technologies that include cancer remediation therapies such as magneto-hyperthermia, magnetic targeted drug delivery, and magneto-rheological fluids, as well as enhanced magnetic resonance imaging.

With reduced dimensionality of nanoparticles and films, and the inherent nonequilibrium nature of many processing schemes, changes in local chemistry and structure have profound effects on the functional properties and performance of ferrites. In this lecture, we will explore these effects upon the fundamental magnetic and electronic properties of ferrites. Density functional theory will be applied to predict the properties of these ferrites, with synchrotron radiation techniques used to elucidate the chemical and structural short-range order. This approach will be extended to study the atomic design of ferrites by alternating target laser-ablation deposition. Recently, this approach has been shown to produce ferrites that offer attractive properties not found in conventionally grown ferrites. We will explore the latest research developments involving ferrites as related to microwave and millimeter wave applications and the attempt to integrate these materials with semiconductor materials platforms.

SCV Consultants' Network of Silicon Valley

TUESDAY September 18

Joint Venture Risks

Speaker: Kevin Roe, Esq., Law Offices of Kevin Roe
Time: Presentation at 7:00 PM
Cost: none
Place: KeyPoint Credit Union, 2805 Bowers Ave., Santa Clara
RSVP: not required
Web: www.CaliforniaConsultants.org

Kevin Roe is an Intellectual Property and Business Attorney in Campbell. He teaches intellectual property law and business law in the evenings for Stanford University. He has taught practical law classes at several other Bay Area colleges, the Sunnyvale Patent Library and for other IEEE groups for many years.

Kevin also serves clients on a wide range of prosecution and litigation issues regarding patents and other intellectual property, technology licensing, contracts, employment law, business formation, business regulations and executive governance, and corporate business disputes. He received a JD from Santa Clara University, a Ph.D. in Electrical Engineering from the University of California and an MS in Electrical Engineering from Stanford University.

Many Bay Area companies and startups are at some point approached with attractive proposals for a joint venture. These typically come from foreign companies, and they frequently have disastrous results. This talk will cover the risks of joint ventures, list some of the danger flags, suggest practical ways to minimize the risks and offer suggestions regarding exclusive licensee risks.

Topics covered will include the following:

* potential types of risk
* potential scenarios
* some simple precautions
* helpful contract provisions
* applicable legal provisions and statutes
* some possible remedial actions

This seminar will be very relevant and useful to technical people and business people directly or indirectly involved in a proposed or future joint venture.

WEDNESDAY September 26

Formation of a Warranty Chain Management Institute and its Applicability for Reliability Engineers

Speaker: Glen Griffiths, Hewlett Packard
Time: Refreshments at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: HP-Cupertino Oak Room, Bldg 48, Pruneridge Ave. and Wolfe Rd., Cupertino
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/rl/events.htm

Warranty costs in the US alone run in the region of $28B per annum [ref - Warranty Week, 3rd March 2007 edition]. Reliability Engineers have a significant influence on the failure rates of equipment, which is a key driver of warranty events and hence cost. Glen will outline the path he has taken, beginning with an investigation into how to improve reliability engineering practices in Hewlett Packard, that led to the creation of a new Warranty Conference series and culminated in the formation of the Institute of Warranty Chain Management (iWCM), of which he is currently President. Along the way, he will discuss the iWCM's applicability and usefulness to reliability Engineers and introduce the Director of the Warranty Chain Management Conference series, Alison Griffiths.

Glen Griffiths is the director of Hewlett Packard's Global Engineering Services responsible for providing engineering and regulatory support across all HP hardware businesses. He manages over 180 people spread across 24 countries with his teams supporting over $60B of products sales annually.

Glen's professional experience has centered on electrical, avionic and reliability engineering as well as systems engineering. Glen retired from the UK Royal Air Force, after serving 22 years as an Engineering Officer. In his previous roles he was operations manager for a squadron of Jaguar strike attack aircraft, managed the software development and test teams for the Harrier aircraft (AV8B) fleet and managed a multi-national team of software reliability and engineering R&D advisors for the Typhoon aircraft. During his last 3 years in the military he was responsible for setting Reliability & Maintainability requirements for all United Kingdom Military Air systems procurement and he also acted as the UK reliability specialist advisor to the US Department of Defense Joint Strike Fighter Project.

Glen holds a Masters in Business Administration, a Masters in Reliability and Maintainability Engineering and an Honors degree in General Engineering. He is a Chartered Engineer in the IEEE and also holds the position of President of the Institute of Warranty Chain.

SF & OEB Power Engineering

THURSDAY September 27

Recent Trends in Substation Automation and Enterprise Data Management

Speaker: John D. McDonald, P.E., Vice President for Power System Automation, KEMA, Inc.
Time: 6:00 PM
Cost: TBD
Place: Scotts Seafood, Jack London Square
RSVP: For information and reservations please email Carole Pharr at carole.pharr@salasobrien.com or call (408) 282-1500 x213.
Web: www.e-grid.net/docs/0709-oeb-pes.pdf

John D. McDonald, P.E., Vice President, Automation for Power System Automation for KEMA, Inc., is assisting electric utilities in substation automation, feeder automation, SCADA/DMS/EMS systems, and communications protocols. He received his B.S.E.E. and M.S.E.E. (Power Engineering) degrees from Purdue University, and an M.B.A. (Finance) degree from the University of California-Berkeley. He is a Fellow of the IEEE, President of the IEEE Power Engineering Society (PES), and Past Chair of the IEEE PES Substations Committee. He has published 31 papers and co-authored three books, including being Editor-in-Chief, and Substation Integration and Automation Chapter author, for the book Electric Power Substations Engineering, Second Edition, published by Taylor & Francis/CRC Press in 2007.

The purpose of this talk is to familiarize participants with all aspects of substation automation. The term Intelligent Electronic Device (IED) is defined. The different levels of substation integration and automation are discussed. The reasons a utility would need substation automation are presented. The components of the integration and automation architecture are discussed with respect to their technical issues. This discussion flushes out the sensitive, controversial issues that need to be addressed by a utility when implementing substation automation. The characteristics and interface issues associated with Intelligent Electronic Devices (IEDs) is addressed, since the integration architecture is only as good as the integration capabilities of the IEDs themselves. Communication protocol fundamentals and considerations are discussed. Relevant industry standards and their impact on substation automation are described. The characteristics of extracting the valuable data from substation Intelligent Electronic Devices (IEDs) and effectively managing this data in the electric utility enterprise is illustrated.

SCV Magnetics

TUESDAY October 16

Imaging Magnetic Surfaces with Atomic Resolution

Speaker: Dr. Matthias Bode, Argonne National Laboratory
Time: Cookies and drinks at 7:30 PM; Presentation at 8:00 PM
Cost: none
Place: KOMAG, 1710 Automation Parkway, San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/mag

Matthias Bode received the diploma in physics from the Free University of Berlin, Germany, in 1993, and the Ph.D. degree in physics from the University of Hamburg, Germany, in 1996. Based on his works on spin-polarized scanning tunneling microscopy he received the habilitation in experimental physics from the University of Hamburg in 2003.

Since 1996 he is a Research Staff Member at the Institute of Applied Physics at the University of Hamburg. In 2007, he joined the Argonne National Laboratory, and is leading the Electronic and Magnetic Materials & Devices Group. In the past 10 years Dr. Bode developed spin-polarized scanning tunneling microscopy, a magnetic imaging technique with a resolution down to the atomic limit. His research explores correlations between structural, electronic, and magnetic properties of epitaxial nanostructures with a special interest in frustrated antiferromagnetic surfaces, superparamagnetism, and new magnetic phenomena.

Dr. Bode has published more than 80 peer-reviewed papers, three review articles, and three book chapters. In 2003 he was awarded the Philip-Morris Award for research.

Fueled by the ever increasing data density in magnetic storage technology and the need for a better understanding of the physical properties of magnetic nanostructures, there exists a strong demand for high resolution, magnetically sensitive microscopy techniques. The technique with the highest available resolution is spin-polarized scanning tunneling microscopy (SP-STM) which combines the atomic resolution capability of conventional STMs with spin sensitivity by making use of the tunneling magneto-resistance effect between a magnetic tip and a magnetic sample surface. Beyond the investigation of ferromagnetic surfaces, thin films, and epitaxial nanostructures with unforeseen precision, it also allows the achievement of a long-standing dream: the real space imaging of atomic spins in antiferromagnetic surfaces.

The lecture addresses a wide variety of phenomena in surface magnetism which in most cases could not be imaged directly before the advent of SP-STM. After starting with a brief introduction of the basics of the contrast mechanism, recent major achievements will be presented, like the direct observation of the atomic spin structure of domain walls in antiferromagnets and the visualization of thermally driven switching events in superpara-magnetic particles consisting of a few hundreds atoms only. To conclude the lecture, recently observed complex spin structures containing 15 or more atoms will be presented.