June 2008

CHAPTER MEETINGS

SCV-Mag - 5/27 | Spintronic Biochips for Biomolecular Recognition - detecting geometries, limits using spin valve... [more]
SCV-PES - 5/27 | 'Leading Indicators' for More Effective Life Testing - anticipating dangerous field failures with a few units... [more]
SF-IAS - 5/27 | Advances in Power System Protection and Automation - microprocessor-based technology... [more]
SCV-CE - 5/27 | Java Technology: The Future of Digital Television - DTV apps and services for broadcast, cable, satellite, IPTV... [more]
OEB-Mag - 5/30 | Spintronic Biochips for Biomolecular Recognition - for portable, point-of-care, diagnostic applications... [more]
SCV-SPS - 6/2 | Enhancing Image Fidelity through Spatio-Spectral Design for Color Image Acquisition, Reconstruction, Display. [more]
SCV-LEOS - 6/3 | Advanced Microscopy Techniques and Ultrafast Lasers: a Symbiotic Development - non-linear optics... [more]
SCV-RAS - 6/4 | Adaptive Control for Autonomous Underwater Vehicles - AI planning for Autonomous Underwater Vehicle... [more]
SCV-EDS - 6/4 | Development of a Technology Platform for Nanoscale RF SoC Design - new effects, issues, further challenges... [more]
SCV-TMC - 6/5 | The Year of Living Dangerously: Extraordinary Results for an Enterprise Agile Revolution and Globalization. [more]
SCV-Mag - 6/10 | Integrated On-Chip Inductors Using Magnetic Material - CoZrTa alloy up to 9.8 GHz, uniaxial anisotropy... [more]
SCV-CPMT - 6/11 | Thermal Stress Modeling in Electronic and Photonic Engineering: Is FEA the Only Tool? - role, attributes. [more]
SCV-PACE - 6/11 | Congressional Insights & Senior Member Upgrade Information Session – innovation, competitiveness... [more]
SF-PES - 6/11 | Past, Present and Future of Solar Thermal Generation - central receiver, parabolic trough, dish Stirling... [more]
SCV-ComSoc - 6/11 | MobileTV/Video Workshop - more details on website... [more]
SCV-Nano - 6/17 | Hybrid Organic-Inorganic Devices Using Self-Assembly Techniques: Application To Solar Cells... [more]
SF-PACE - 6/17 | Engineering Your Presentation: Speaking Skills - better communication techniques... [more]
SCV-ComSoc - 6/19 | Location-Based Technologies and Services - location as a utility; because life moves... [more]
SCV-SSC - 6/19 | WiMedia Ultra-Wide-Band Communication - high-rate short-range communications in the 3.1 to 10.6 GHz range... [more]
OEB-IAS - 6/19 | Power System Grounding - IEEE Standard 141; hybrid high-resistance grounding systems... [more]
SCV-PSES - 6/24 | Sustainability - What It Means to Product Safety Engineers and Why They Should Care - renewable energy... [more]
SCV-CS - 7/19 | Cloud Computing: The New Face of Computing - Promises and Challenges - hosting email, calendars online... [more]

Conference Calendar

June 2-4: IEEE Conference on System of Systems Engineering - Portola Plaza Hotel, Monterey [more]
June 5-6: The Industrial Electronics Industry Forum - Santa Clara Marriott [more]
June 8-13: Design Automation Conference (DAC) - Anaheim Convention Center - Register by May 19 [more]
June 16-20: Conf on Sensor, Mesh and Ad Hoc Communications and Networks (SECON 2008) - Crowne Plaza Hotel, Burlingame Deadline: June 1 [more]
June 18-20: ASME Frontiers in Biomedical Devices Conference - Hyatt Regency, Irvine [more]
Aug 4-7: IEEE Conference on Semantic Computing - Santa Clara Marriott [more]
Aug 12-14: 3rd Annual Flash Memory Summit - Santa Clara Marriott [more]

CALLS FOR PAPERS:


Professional Skills Courses
- Speed Reading - Budgeting Essentials
- Agile Project Management for SW Developers

Technical Skills Courses/Seminars
- Design of RF Integrated Circuits and more

Santa Clara University: Info Sessions
Open University summer courses – a chance to try it out

Positions Available:
Senior Electrical Engineer
MK2 Engineering, Napa Valley [more]
Associate Electrical Engineers
East Bay Municipal Water District [more]
UC-Santa Cruz Extension - Instructors [more]

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MARKETPLACE – Services page 3
From the Editor’s Desk ...

Last week I attended a Users Group session for subscribers to IEEE’s very large Xplore research database. Many of the region’s largest university libraries, as well as other research labs and companies, were represented.

It takes considerable resources and development effort to maintain and advance the search capabilities, content, and usefulness of a large system such as this one. I heard many suggestions for improvements, as librarians and researchers described how their users accessed the content. Improvements to the user interface were suggested and noted. The Xplore search engine and interface are being updated at the end of the year to version 3.0, with additional capabilities and services.

All engineers (whether IEEE members or not) are encouraged to use Xplore (at ieeexplore.ieee.org). Chances are good that your employer or university has a subscription, allowing you full access to the collection. And if not, then you can still do basic searches and browse the collection (though perhaps not download PDFs of the actual papers).

Paul
Do you provide a service? Would you like more inquiries?

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- Monthly and Annual Rates available

Visit our Marketplace (page 3)

Download Rates and Services information:
www.e-grid.net/docs/marketplace-flyer.pdf
Fifth Annual IEEE Communications Society
Conference on Sensor, Mesh and Ad Hoc Communications and Networks (SECON 2008)

June 16-20, 2008
Crowne Plaza SFO Airport, Burlingame

IEEE SECON provides a forum for the exchange of ideas, techniques, and applications, for discussion of best practices, to raise awareness, and to share experiences among researchers, practitioners, standards developers and policy makers working in sensor, ad hoc, and mesh networks and systems.

Original technical papers are presented on the communications, networking, applications, systems and algorithmic aspects of mesh and sensor networks, as well as on practical deployment and implementation experiences.

Corporate Sponsors:

Co-Sponsor: Santa Clara Valley Section, IEEE

SILICON VALLEY TECHNICAL INSTITUTE

Upcoming Courses with labs

Design of Radio Frequency Integrated Circuits
12 week course, M/W 6:00PM-9:00PM (Starts: May 19)
A balance of communications, physics and IC design. Includes high-speed amplifiers, LNA, Mixer, VCO, PA, PLL and other RF blocks.

PCB Design Fundamentals for Analog and RF
12 week course, T/Th 6:00PM-9:00PM (Starts July 15)
For engineers or managers who want learn basics of DFT techniques and theory: Fault Models, Levels of Abstraction, Test Approaches, Scan Design Rules, Test Generation Methods, BIST, Analog and Mixed Signal Testing, more.

MATLAB & Simulink for Design & Digital Signal Processing
12 week course, T/Th 6:00PM-9:00PM (Starts August 26)
Hands-on, from basic concepts in discrete time systems, filter design and implementation all the way to advanced concepts of multi-rate systems; balanced mix of theory and practice.

Discount of $40 for IEEE Members on 12-week courses.

Keynote: “Reuniting Wireless Sensor Networks with the IP Architecture,” David E. Culler, UC-Berkeley

Technical Sessions: (Tues-Thurs, June 17-19)
- Localization and Location Management
- Routing and Topology Management I & II
- Energy Efficient Protocols
- Software and Hardware
- Medium Access Control
- Theoretical Foundations
- Transport Layer Issues
- Sensor Coverage
- Data Fusion and Processing
- Time Synchronization and Cooperative Protocols
- Vehicular Networks, Emerging Areas and Novel Applications
- System Deployment and Experiences
- Analytical Models
- Security and Privacy
- Cross Layer Design

Workshops: (held on Monday, June 16)
- Third IEEE Workshop on Wireless Mesh Networks
- Third IEEE Workshop on Networking Technologies for Software Defined Radio (SDR) Networks
- First IEEE Int’l Workshop on Wireless Network Coding

Earlybird rates through June 1

For more information and to register:

www.ieee-secon.org

Upcoming 1- and 2-day Seminars:

June 19-20: Advanced Semiconductor Technology & Fabrication

June 26-27: Wireless Communications with Matlab and Simulink: IEEE802.16 (WiMax) Physical Layer

Sept 4: Biomedical Technologies - Opportunities & Challenges

Sept. 5: Device & Interconnect Reliability in Advanced CMOS

Discount of $30 for IEEE Members on Seminars.

Get more information on all upcoming classes:

www.svtii.com/SVTI-calendar.htm

Review all SVTI offerings: www.svti.org
MK2 Engineering, Inc. has an excellent opportunity for an experienced electrical engineer to join our growing electrical team. Located in the world-famous Napa Valley, we are a consulting engineers firm specializing in innovative, energy-efficient design of HVAC, plumbing, electrical and fire protection systems.

MK2 is currently searching for a Senior Electrical Engineer to provide leadership for our growing electrical department. This is an outstanding opportunity to work for a stable company that offers a chance to grow with a firm that has continued to expand during the last nine years.

As a Senior Electrical Engineer, you will be expected to effectively coordinate projects, review quality of the design product, design electrical systems and organize staff supporting your efforts. Responsibilities include managing all aspects of electrical design projects including: load calculations, lighting and power system design, short-circuit calculations, system selection, equipment selection, specifications, design, layout, field visits and construction administration. You will be responsible for oversight of profitability and timeliness of production; support of the design and engineering of electrical systems for new installations, system retrofits, system replacement, and system upgrades. As an Electrical Engineer you must have a thorough familiarity and understanding of emergency generators, UPS, fire alarm design, and co-generation systems.

As a department leader you will be in charge of the quality and the quantity of electrical engineering design products. The engineering staff under your charge will provide engineering solutions and project management for our projects in wineries, schools, commercial, institutional and health care facilities.

Technical Qualifications:
Minimum 10 years of Electrical Engineering experience with a US consulting engineering firm(s)
BSEE degree from accredited university
California PE license required
Minimum 3 years of project management and staff supervision
Knowledge of California, Title 24 Energy Standards
Thorough knowledge of NEC and NFPA
LEEP AP or the ability to become accredited
Excellent written and verbal communication
Proficient in Microsoft Office (Word, Excel…)

How to apply:
Send cover letter and resume to resume@mk2eng.com
In subject line please note “re: Sr.Electrical Engineer” or fax to (707) 307-1550.

For a profile of our company, please visit www.mk2eng.com
For further information, contact Jason Mueller, JMueller@MK2Eng.com

**POSITIONS: ASSOCIATE ELECTRICAL ENGINEER**

**EAST BAY MUNICIPAL UTILITY DISTRICT**

There are two permanent openings located in the Design Division of the Engineering and Construction Department and in the Support Services Division of the Wastewater Department. Both report to Senior Electrical Engineers. For these openings, strong technical expertise in power system engineering with some experience in control systems and instrumentation engineering is highly desirable.

Requirements:
- A bachelor’s degree in an ABET-accredited electrical engineering curriculum (OR a California EIT Certificate)
- Four years of professional electrical engineering experience
- Current CA registration as a Professional Electrical Engineer.

Advance your career as an Associate Electrical Engineer with an industry-leading water supply and wastewater utility.

Salary range: $91,764 to $111,528, plus exceptional benefits.

Read the complete position description: [www.e-grid.net/docs/0805-ebmud.pdf](http://www.e-grid.net/docs/0805-ebmud.pdf)

If you meet the qualifications and believe you fit the Ideal Candidate Profile, please complete and submit both a District application and the required supplement by Friday, June 6, 2008.

For full details and application materials, visit us at [www.ebmud.com](http://www.ebmud.com)

ICSC is an interdisciplinary forum for researchers and practitioners to present research that advances the state of the art and practice of Semantic Computing, as well as to identify the emerging research topics and to define the future of Semantic Computing. The conference particularly welcomes interdisciplinary research that facilitates the ultimate success of Semantic Computing.

The field of Semantic Computing brings together disciplines concerned with connecting the intentions of humans with computational content: retrieving, using and manipulating existing content according to user's goals; and creating, rearranging, and managing content that matches the author's intentions. The technical program of ICSC2008 includes tutorials, workshops, invited talks, paper presentations, panel discussions, demo sessions, and an industry track.

**Two Panels:**
Getting Traction and Not Skid Marks: The Rubber Meets the Road
Semantic Computing: Issues, Challenges, and Future Research Directions

**Special Sessions:**
- Scalability in Semantic Computing: the European View
  - Semantic Service Orientation
  - Semantic Middleware
  - Semantic Web Reasoning
  - Identity and Reference Management
- Semantic Analysis of Tactical Chat
  - Robustness on high-jitter networks
  - Migration to XMPP-based chat
  - For edge, tactical users
- Mobile Semantic Computing
  - Bandwidth constrained environments
  - Utilization of semantic annotation
  - Role of semantic web for social computing, Web 2.0

**Six Tutorials:**
- Text Analytics for Semantic Computing - the good, the bad and the ugly
- Enhancing Semantic via Knowledge Discovery from Distributed Multimedia Information Systems
- Introduction to Ontology, RDF, and OWL
- Semantic Business Process Management
- Inductive Logic Programming for the Semantic Web
- Utilizing Federated Knowledge in Semantic Web Apps

More information, and to register:
[icsc.eecs.uci.edu](http://icsc.eecs.uci.edu)

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**Engineering Your Presentation**

Speaking Skills: Do You Have Them Under Control?
Presented by San Francisco Section PACE
June 17, July 1 & July 15 (Different Topics each Session)
Time: 6:30 – 8:30 PM  Downtown Oakland

While technically expert in their field, often engineers are not proficient at public speaking. Successful communication of ideas through speech requires disciplines similar to engineering but with differing techniques. Ashley Harkness has faced this challenge numerous times. Over this set of 2-hour seminars, Mr. Harkness will explore better communication techniques by addressing the issue of how to "Engineer Your Presentation." Topics to be covered include:

• Constructing your Speech
• Making a Photo Really Say 1,000 Words
• Presentation Success
• Group/Panel Discussions: Keeping Your Sense of “Self”
• Keeping it “Real”
• Speaking Notes, A Road Map and, Maybe, Your Next Book

Other topics covered:
• Effective Power Point and Your Audience
• When Handouts are the Only Way
• Extemporaneous Speaking: The Elevator, your Boss, the Project, and he wants to know
• Presenting that Paper: bringing life to your subject

IEEE Members: $20  Non-Members: $60
Prices includes all 3 Sessions!  RSVP Required
Registration Deadline: June 13
Contact Dan Sparks, [dan.sparks@ieee.org](mailto:dan.sparks@ieee.org)

For the full flyer:
[www.e-grid.net/docs/0806-sf-pace.pdf](http://www.e-grid.net/docs/0806-sf-pace.pdf)
We invite highly qualified instructors to apply to teach, as well as submit course proposals. Share your knowledge and mentor new engineers. Be a leader in the field and develop networking. Current areas of interest include:

- High-speed IO Design
- PrimeTime Signal Integrity
- WiMax, CDMA, Quality of Service
- Mobile Device, Gaming, Digital Video
- Parallel and Concurrent Programming
- Software Security, Device and Web Security
- Java Enterprise Edition 5
- C#, .NET Development Environment

The IES Industry Forum
5-6 June 2008
Marriott Hotel, Santa Clara

Industrial and embedded technologies are expanding in industry settings, and in other markets such as robots in the home, sensors in the car, etc. The Internet has allowed devices to advance from isolated objects to being remotely controlled. This combination makes exciting discussions among computing, communications and industrial technologies experts. This Forum focuses on elements to build and use Industry Systems, the business directions for industry technologies, security requirements, and industry research.

Session 1: Trusting Industry Computing
Led by a keynote from Victoria Stavridou-Coleman, Samsung Computer Science Laboratory VP, this session looks at the security and reliability requirements for Industry Computing. Speakers: Jean-Pierre Seifert, Samsung; Michael Condry, Intel. A look at three outcomes: must have it, it’s a pain but maybe needed, and finally forget it – it’s nonsense.

Session 2: Building for Industry Computing

Evening Reception: networking with colleagues, speakers.
Flash memory is a key technology enabling new designs for many products in the consumer, computer and enterprise markets. The Flash Memory Summit is the only place where you will hear the people who are making these products happen! Network with companies and people that will create the next generation of hardware and software.

This power-packed 3-day event will cover the latest topics in Flash Memory. Get the latest from leaders in the field on: Flash in computers and enterprise, cards and SSDs, flash controllers, improvements in storage capacity and reliability, designing with flash memory, new non-volatile storage technologies, Customer Talks Back session, and more!

Topics of Interest

- Design methods, best practices, emerging standards
- Flash software, controllers, and formats such as SD cards, USB drives, flash disks, mobile handsets
- Embedded applications
- Consumer applications
- Hybrid systems (disk or DRAM)
- Storage security and programming requirements
- SDDs in computers, computer applications and flash-based microcontrollers

Participating Companies include Intel, Samsung, Micron, Adtron, SanDisk, MOSAID and many more.

Who Should Attend?

- Designers of hardware, software, consumer electronics, memory and embedded systems
- Applications, storage, communications, computer, systems, and test engineers
- Storage specialists
- Engineering managers, systems analysts, solution providers and consultants
- VARs, OEMs, system integrators, venture capitalists, marketing and product managers

Keynote Speakers

- Eli Harari, SanDisk
- Dean Klein, Micron
- Knut Grimsrud, Intel
- Ed Doller, Numonyx
- Jim Elliott, Samsung

Proposals for presentations are due by June 13

Please contact Lance Leventhal (+1-858-756-3327) with your proposed topic:
lance@flashmemorysummit.com

For more information, and to register online:
flashmemorysummit.com

Free parking
The main conference program for POF2008 will be held from Tuesday, August 26th, to Thursday, August 28th, with exhibits open during the conference. Tutorials covering a wide range of POF topics are on Monday, August 25th.

A three-day summer POF workshop the week before offers the US audience a chance to learn from Europe’s POF know-how.

Organized by

Santa Clara University School of Engineering Graduate Programs

SCU Summer Open University

Have you ever wanted to continue your education in engineering while you continued working? Santa Clara University’s School of Engineering offers graduate degree and non-degree programs to both full-time students and working professionals. Simplified registration for the Summer Open University. Graduate-level instruction. Up to 12 units may be transferred to a graduate-degree program.

**Early-morning classes:**
- Linear Algebra
- Operating Systems Case Study
- Applied Mathematics
- Parallel Programming
- Logic Design Using HDL (and more)

**Evening classes:**
- Global Technology Development
- Hardware Formal Verification
- Logic Design Using HDL
- IC Fabrication Process
- Nanoelectronics (and more)

**Saturday classes:**
- Global Software Management
- Next Level Leadership
- Advanced Project Management
- Law, Technology, IP

Email Wan Chen with inquiries: WQChen@scu.edu

**Call for Papers:**
Abstracts are solicited through June 1, in the following areas:

**Technology:**
- Cables
- Connectors
- Couplers
- Detectors
- Environmental Testing
- Fiber Bragg Gratings
- Hardware
- High-Temperature Components
- Illumination
- Materials
- Multimode GI Fibers
- Microstructured Fibers
- Sensors
- Standards
- Step index Fibers
- Transceivers
- Test and Measurements
- Tools
- WDM Components

**Applications:**
- Aircraft & Aerospace
- Automotive
- Building Wiring
- Consumer Electronics
- Data Centers/Servers Farms
- Embedded Woven in Fabrics
- Home Networks
- Industrial Controls
- Interconnects
- IPTV
- Local Area Networks (LAN)
- Medical
- Military
- Sensor Applications
- Signs & Illumination
- Storage Area Networks (SAN)
- Supercomputer Interconnects
- Surveillance Systems
- Wireless Backbones

Abstracts due June 1 – Submit online at www.POF2008.com

Save $100 through August 1! Group discounts.

Located in the heart of Silicon Valley, with easy parking.

**Choice of three Sessions:**
- Session I - 10-week classes (June 16 - August 22)
- Session II - 5-week classes (June 16 - July 18)
- Session III - 5-week classes (July 28 - August 29)

… plus a number of one-day Saturday classes

To learn more, attend a Wednesday early-evening information session on June 4 or June 25: Visit www.scu.edu/engineering/graduate/event_rsvps.cfm

Review summer Open University courses:

www.scu.edu/engineering/graduate
IEEE Professional Skills Courses

**Speed Reading**
- Date/Time: Thurs, June 5, 8:30AM – 3:30PM
- Location: – eBay, Inc., San Jose
  Fee: $400 for IEEE Members; $500 non-members
"Kathleen's knowledge of subject matter was excellent. I was able to see immediate results from all the different exercises throughout the day."
-Engineer, Cypress Semiconductor

**Influential Communication**
- Date/Time: Tues, June 10, 8:30AM – 4:30PM
- Location: – TIBCO Software, Palo Alto
  Fee: $400 for IEEE Members; $500 non-members
"Excellent content - useful and actionable."
-Head of Marketing Solutions & Ops, eBay, Inc.

**Budgeting Essentials**
- Date/Time: Wed, July 9, 8:30AM – 12:30PM
- Location: – Synopsys, Mountain View
  Fee: $300 for IEEE Members; $350 non-members
"Very good! Particularly helpful for management, but also useful to know and understand for individual contributors."
-Test Engineer, Cypress Semi

**Management Essentials**
- Date/Time: W/Th, July 9-10, 8:30AM – 4:30PM
- Location: – TIBCO Software, Palo Alto
  Fee: $625 for IEEE Members; $700 non-members
"Thank you!! I wish I could have had this knowledge along time ago when I first became a supervisor."
-Sales Operations Supervisor, @Road

**Virtual Teams: Working Together Apart**
- Date/Time: Thurs, July 17, 8:30AM – 4:30PM
- Location: – Cypress Semiconductor, San Jose
  Fee: $400 for IEEE Members; $500 non-members

NEW! Agile Project Management for Software Developers
- Date/Time: Tues, June 17, 8:30AM – 4:30PM
- Location: – TIBCO Software, Palo Alto
  Fee: $525 for IEEE Members; $600 non-members
This workshop teaches the fundamentals of agile project management, and is recommended for everyone who will be involved in an agile software project. We will explore the key roles, responsibilities, interactions, and processes that make a successful agile project happen. The workshop focuses on practical 'how to' skill development, while providing enough theory so that participants will understand why the techniques work. See also the June 5th TMC meeting on the www.e-grid.net website.

Preparing Technical Content for Presentation
- Date/Time: Thurs, July 24, 8:30AM – 4:30PM
- Location: – Synopsys, Mountain View
  Fee: $400 for IEEE Members; $500 non-members
"The nine-step preparation process is extremely valuable with delivery of presentations."
-Hewlett Packard

Influential Communication
- Date/Time: Tues, Aug 5, 8:30AM – 4:30PM
- Location: – Synopsys, Mountain View
  Fee: $400 for IEEE Members; $500 non-members

For complete course information, schedule, and registration form, see our website: www.EffectiveTraining.com

Improve your skills – register for one of these classes, or for others coming up this summer. Bring a team!
DAC is the premier event for the electronic design community. It offers the industry’s most prestigious technical conference in combination with the biggest exhibition, and brings together design, design automation and manufacturing market influencers. Industry leaders, market leaders, technical leaders, business leaders and thought leaders all converge at DAC. The DAC technical program is made up of 14 tutorials, 7 workshops, 8 topical panels, a slate of Pavilion panels and 36 technical sessions divided into 12 Topical Areas, plus keynotes and exhibits.

Management Day: (all-day Tuesday)
Providing managers with timely information to help make decisions where business and technology intersect. The day is comprised of three sessions featuring presentations by managers representing key independent device manufacturers (IDMs) and major fabless companies.

Keynote Speakers:
EDA for Digital, Programmable, Multi-Radios  
Justin R. Rattner, Chief Technology Officer, Intel Corp.
Challenges on Design Complexities for Advanced Wireless Silicon Systems  
Sanjay K. Jha, President, Qualcomm CDMA Technologies
Idea to implementation: A Different Perspective on System Design  
Jack Little, President, The Mathworks

Colocated Events:
June 8-9: IEEE Symposium on Application Specific Processors (SASP 2008)
June 8-9: IEEE Symposium on Application-Specific Processors
June 9: IEEE Int’l Workshop on Hardware-Oriented Security and Trust (HOST-2008)

Special Topical Areas:
• Synthesis and FPGAs  • Interconnect and Reliability  • DFM & the Mfg Interface  • Analog/RF/Mixed Signal & Simulation
• Verification & Test  • Physical Design  • Low-Power Design
• New/Emerging Technologies  • Wireless  • Strictly Design
• System-level and Embedded  • Business

45th DAC Workshops  (Sunday and Monday)
• High-level Synthesis: Back to the Future  • UML for SoC Design Workshop  • Biochips to Interface and Monitor Human Biological Functions  • System and SoC Debug Workshop  • Design and Verification of Low Power SoCs: An Application Oriented Approach  • Low Power Coalition Workshop - Advances in Low Power Design for Circuits and Systems  • Cross-layer Power and Thermal Management
• Diagnostic Services in Network-on-Chips (DSNOC)
• Introduction to Chips and EDA for a Non-technical Audience  • Women in Design Automation: Achieving Career Balance in an Unbalanced World  • OpenAccess: A Platform for Continuous Evolution and Innovation  • Integrated Design Systems Workshop  • Diagnostic Services in Network-on-Chips (DSNOC)  • Beyond Syntax and Semantics: Industry Experiences with OVL/SVA/PSL

Tutorials:
Bridging a Verification Gap: C++ to RTL for Practical Design  • Programming Massively Parallel Processors: the NVIDIA Experience  • Robust Analog/Mixed-signal Design  • DFM Revisited: A Comprehensive Analysis of Variability at all Levels of Abstraction  • Low Power Techniques for SoC Design  • System Level Design for Embedded Systems

Plus 6 Hands-on Tutorials with the theme “Embedding intellectual property in your design: challenges & solutions”

Substantial discount for IEEE and ACM members, students

Access the Advance Program on the website:
www.DAC.com
June 2-4, 2008
Portola Plaza Hotel and Spa
at Monterey Bay

Conference Theme: **SoSE in service of Energy and Security**

SoSE 2008 provides a world-class forum for all aspects of systems engineering, human-machine systems and emerging cybernetics, with their vast ramifications in numerous engineering fields such as control, computing, communications, information technology and applications to manufacturing, defense, national and homeland security, aerospace, aeronautics, energy, and the environment.

**2008 Workshop: International Consortium on System of Systems (ICSOS)**
June 5, 2008

Workshop Theme: **SoS and SoSE in service of Security, Energy and Environment**
www.icsos.org/2008workshop

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**Keynote Talks:**
- Challenges in Undersea Warfare Systems of Systems
- Systems Engineering & Management of System Families
- System of Rovers and their Application
- OMG Systems Modeling Language
- Global Earth Observation System of Systems – Is the Palnet Earth ready for the Next Tsunami?
- Extending B-787 E-Enabling SoS to Other Means of Transportation
- IEEE-INCOSE Relations on SoSE

**Sessions:** Over 100 short presentations

Plus exhibits

**For additional information:**
www.ieeesose2008.org

Sponsored by the IEEE Systems, Man, and Cybernetics Society and the IEEE Systems Council
Point of contact: Mo Jamshidi, moj@wacong.org

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**An information-packed three day Symposium on the latest in High Performance Interconnects, **IEEE Hot Interconnects** brings together architects and designers of high-performance chips, software, and systems at the University and global business levels. Presentations focus on the latest technological developments of the leading engineers and researchers in the field.**

**Topics Addressed:**
- Novel and innovative interconnect architectures
- Multicore processor interconnects
- System-on-Chip Interconnects
- Advanced chip-to-chip communication technologies
- Optical interconnects
- High-speed packet processing engines and network processors
- System and storage area network architectures and protocols
- High-bandwidth and low-latency I/O
- Tb/s switching and routing technologies
- Novel communication architectures to support grid computing

**August 26-28, 2008**

The Symposium focuses especially on real experimental systems, prototypes, and leading-edge products and their performance evaluation. Themes include cross-cutting issues spanning computer systems, networking technologies, and communication protocols.

The 2008 HOT Interconnects Symposium invites experts to present half-day tutorials on topics of interest, at an introductory or overview level. For more information: tutorials@2008.hoti.org

More information:
www.hoti.org

Save through August 13th
Free on-campus parking
Integrated spintronic biochip platforms are being developed for portable, point-of-care diagnostic applications. The platforms consist of a microfluidic unit where the bioassay takes place, an arraying and detector chip consisting of target arraying current lines and integrated magnetoresistive sensors, and electronic control and readout boards. Probe biomolecules are immobilized by microspotting over sensor sites, and target biomolecules, labeled with magnetic nanoparticles, are arrayed over the probe sites (magnetically assisted hybridization). After proper washing, hybridized targets are recognized by the fringe fields created by the magnetic beads, and detected by the incorporated magnetoresistive sensors. Detecting geometries will be reviewed, using either out-of-plane or in-plane bead excitation, and dc or ac detection/excitation. Detection limits using spin valve and tunnel junction sensors will be presented, depending ultimately on platform electronic noise, and sensor noise characteristics. Applications to gene expression chips (Cystic Fibrosis gene mutation detection) and immuno assay chips (anti-body-antigen recognition, e-Coli, Salmonella detection) will be presented. Spintronic biochips are also being integrated into multi-module lab-on-chip platforms including:

1. biomolecule extraction from biological fluids (magnetophoresis),
2. PCR modules (if required), and
3. the biomolecular recognition module.

Alternative spintronic biochip geometries will also be presented (lateral flow biosensors), where a magnetoresistive reader scans the surface of a porous strip, where labeled target biomolecules bind to immobilized probes. Finally, a brief review of other biomedical applications of magnetoresistive sensors will be given, from hybrid sensors targeted at biomedical imaging, to magnetic tweezers/sensors for DNA translocation monitoring.

Paulo Freitas is a Full Professor of Physics at the Instituto Superior Tecnico (IST) in Lisbon, and the Director of INESC Microsystems and Nanotechnologies. Current research topics include MRAMS, read heads for ultra high density recording, magnetoresistive biochips, and sensors for biomedical applications. He has been involved in research in the area of magnetoresistive materials and devices since he received his Ph.D in Solid State Physics from Carnegie Mellon University in 1986. His PhD thesis was on the subject of anisotropic magnetoresistance of ferromagnetic thin films and alloys. He then joined IBM Research at Yorktown Heights as a post doctoral fellow working on high-TC superconductivity and transport properties of ferromagnetic thin films. In 1988 he joined INESC in Lisbon, where he started the Solid State Technology Group.

In 1989 he became Professor of Physics at the Instituto Superior Tecnico in Lisbon. From 1992 to 1996, he was responsible for the start up and operation of INESC’s ASIC back-end of the line microfabrication facility. From 1996 till now, his research areas expanded to magnetoresistive read elements for magnetic data storage, magnetoresistive sensors, MRAMS, and biomedical applications including magnetoresistive biochips. He became director of INESC Microsystems and Nanotechnologies in 2001, and Full Professor of Physics at IST in 2002. Over this period, he co-authored over 200 technical papers and several chapter books. Professional activities include membership in IEEE, participation in several Publication/Program/Advisory Committees of MMM and Intermag Conferences.
The recent grounding of flights by American Airlines shows that operational maintenance and potential equipment failures are a serious “real-world” safety concern. Safety standards for power tools also look at failure modes. One way to anticipate field failures is to run life tests.

This presentation describes a new approach to life testing, using “Leading Indicators”, that can help overcome common challenges and constraints, such as:

- Too few specimens and too little time available for life testing.
- Life testing results too late to improve product development.
- Maintenance based on the average status of a population of similar units in similar operation, instead of the real-time status of each specific unit.

Failures are expensive, failures irritate customers, and failures can KILL you …

How can you anticipate dangerous field failures with only a few units to test?
The development of microprocessor-based technology in protective relaying has enabled users to employ these devices in a variety of ways. The “protective relay” has evolved into an “intelligent electronic device” with enhanced functionality in protection and control. The key is for the user to understand the capabilities of these devices so that they can be utilized in ways that maximize return to the organization. We will discuss applications that show these capabilities. These applications may include automation and protection methods to mitigate Arc Flash requirements; innovative control methods that reduce engineering and commissioning requirements; and the enhanced use of tools and information to enhance the troubleshooting of both electrical system and equipment events.

Please join us in welcoming our speaker to San Francisco for what is sure to be an interesting and productive session.

Our speaker is Ron Beltran, a Field Application Engineer for GE Multilin. His responsibilities include product and applications support in power system relaying and automation for utility and industrial customers in the Western U.S.A. Ron has nearly 20 years of experience in Power System Engineering with past work experience at Mobil Oil, Pacific Gas and Electric, and ABB. He is also a Senior Member of the IEEE (PES and IAS) and a Registered Professional Electrical Engineer in the State of California.
Java Technology: The Future of Digital Television

Speaker: Bill Shepard, Sun Microsystems
Time: Social, pizza, drinks at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: Hewlett Packard, Oak Room, 19447 Pruneridge Avenue (Building 48), Cupertino
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/ce

Bill Sheppard is Chief Digital Media Officer for the Client Software Group at Sun Microsystems. Upon joining Sun in 1997 he launched Sun's digital television initiative and has led efforts to craft global standards for next-generation television technology. Mr. Sheppard works with cable and satellite operators, broadcasters, studios and other content providers, device manufacturers, governments, and standards bodies worldwide to drive the architecture, development, and adoption of standards-based digital TV technology. Mr. Sheppard is also a Director of the Blu-ray Disc Association and a member of the Academy of Television Arts and Sciences. Mr. Sheppard, an accomplished trombonist, holds a B.S. in Computer Engineering from Iowa State University.

The talk will discuss how Java technology has emerged as the common platform for developing digital television applications and services for broadcast, cable, satellite, IPTV, and Blu-ray Disc. The talk will include an overview of digital television standards and specifications, current and projected market deployment, and approaches used for authoring DTV content.
Spintronic Biochips for Biomolecular Recognition

Speaker: Prof. P. Freitas, INESC Microsystems and Nanotechnologies, Physics Department, IST, Lisbon, Portugal

Time: Presentation at 1:00 PM

Cost: none

Place: Conference room in Bldg 6 (6-2202), Lawrence Berkeley National Laboratory, 1 Cyclotron Rd, Berkeley

RSVP: Please respond by email by May 21 with name, company, to Peter Fischer, PJFischer@lbl.gov so that we can prepare LBNL badges in advance for you

Web: www.e-grid.net/calendar.html#oeb-mag

Paulo Freitas is a full Professor of physics at the Instituto Superior Tecnico (IST), Lisbon, Portugal, and the director of INESC Microsystems and Nanotechnologies. His current research topics include magnetic random access memory (MRAM), read heads for ultra-high-density recording, magnetoresistive biochips, and sensors for biomedical applications. He has been involved in research in the area of magnetoresistive materials and devices since he received the Ph.D. degree in solid state physics from Carnegie Mellon University in 1986. His thesis was on anisotropic magnetoresistance of ferromagnetic thin film and alloys. He joined IBM Research, Yorktown Heights, NY, as a postdoctoral fellow working on high-temperature superconductivity and transport properties of ferromagnetic thin films. In 1988, he joined INESC, Lisbon, Portugal, where he started the Solid State Technology Group. In 1989, he became Professor of physics at the Instituto Superior Tecnico, Lisbon. From 1992 to 1996, he was responsible for the startup and operation of INESC’s application-specific integrated circuit (ASIC) back-end microfabrication facility. Since 1996, his research areas expanded to magnetoresistive read elements for magnetic data storage, magnetoresistive sensors, MRAM, and biomedical applications including magnetoresistive biochips. He became director of INESC Microsystems and Nanotechnologies in 2001 and full Professor of physics at IST in 2002. Over this period, he co-authored over 200 technical papers and several book chapters. His professional activities include membership in IEEE, and participation in several publication, program, and advisory committees for the Magnetism and Magnetic Materials and Intermag Conferences.

Integrated spintronic biochip platforms are being developed for portable, point-of-care, diagnostic applications. The platforms consist of a microfluidic unit where the bioassay takes place, an arraying and detector chip consisting of target arraying current lines and integrated magnetoresistive sensors, and electronic control and readout boards. Probe biomolecules are immobilized by microspotting over sensor sites, and target biomolecules, labeled with magnetic nanoparticles, are arrayed over the probe sites (magnetically assisted hybridization). After proper washing, hybridized targets are recognized by the fringe fields created by the magnetic beads, detected by the incorporated magnetoresistive sensors. Detecting geometries using out-of-plane or in-plane bead excitation and dc or ac detection excitation will be reviewed. Detection limits using spin valve and tunnel junction sensors will be presented, depending ultimately on platform electronic noise and sensor noise characteristics. Applications to gene expression chips (cystic fibrosis gene mutation detection) and immunoassay chips (antibody-antigen recognition; E. coli, salmonella detection) will be presented.

Spintronic biochips are also being integrated into multi-module lab-on-chip platforms including biomolecule extraction from biological fluids (magnetophoresis), polymerase chain reaction (PCR) modules (if required), and the biomolecular recognition module. Alternative spintronic biochip geometries will also be presented (lateral flow biosensors), where a magnetoresistive reader scans the surface of a porous strip where labeled target biomolecules bind to immobilized probes.

Finally, a brief review of other biomedical applications of magnetoresistive sensors will be given, from hybrid sensors targeted at biomedical imaging, to magnetic tweezers/sensors for DNA translocation monitoring.
Enhancing Image Fidelity through Spatio-Spectral Design for Color Image Acquisition, Reconstruction, and Display

Speaker: Keigo Hirakawa, Postdoctoral Research Associate, Harvard University, Department of Statistics

Time: Fast food and drinks at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation for refreshments
Place: National Semiconductor, north end of Building E, 2900 Semiconductor Dr., Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/sps

Dr. Keigo Hirakawa is currently a postdoctoral research associate at Harvard University, working under Prof. Xiao-Li Meng in the Statistics Department. His current research generalizes image processing techniques to the case when the given image has missing data.

The majority of the image processing algorithms proposed today present engineering solutions to imaging problems. Keigo Hirakawa's multidisciplinary research in model-based signal processing, however, is motivated by mathematical, statistical, psychological, and real-world models. In particular, he is interested in bridging the noticeable disconnect between the current engineering solutions to imaging problems and areas of studies that include statistics, human visual system, color science, and device-specific noise models.

Hirakawa graduated magna cum laude from Princeton University with B.S.E. in electrical engineering, a minor in computer science, and another minor in music performance. He became interested in image processing while interning at NEC Corporation in Japan in 1998, and he helped design digital camera hardware for Hewlett-Packard in 1999.

After graduating from Princeton, Hirakawa began the M.S./Ph.D program at Cornell University. He worked extensively in model-based image processing, including image denoising, methods to combine demosaicing and denoising, and color science. He has been an imaging consultant, lecturer, and research engineer at Texas Instruments.

In the first part of the talk, we consider extending an image denoising problem to the problem of missing or incomplete pixel values --- either due to mechanical designs or distortions. In the context of wavelet-based image processing, missing or incomplete pixels pose a particularly difficult challenge because none of the wavelet coefficients can be observed. In this talk, a unified framework for coupling the EM algorithm with the Bayesian hierarchical modeling of transform coefficients is presented. This empirical-Bayes strategy offers a statistically principled and extremely flexible approach to a wide range of pixel estimation problems including image denoising, image interpolation, super resolution, demosaicing.

In the second part of the talk, we consider the "throughput" of color imaging systems. Pixel values are typically sensed or displayed via a spatial subsampling procedure implemented as a color filter array --- a physical construction whereby only a single color value is measured or displayed at each pixel location. Owing to the growing ubiquity of acquisition and display devices, much of recent work has focused on the implications of such arrays for subsequent digital processing, including in particular the canonical demosaicking task of reconstructing a full color image from spatially subsampled and incomplete color data acquired under a particular choice of array pattern. In contrast to the majority of the acquisition and display literature, we consider here the problem of color filter array design and its implications for spatial reconstruction quality. We prove the sub-optimality of a wide class of existing array patterns, and provide a constructive method for its solution that yields robust, new panchromatic designs implementable as subtractive colors.

(Biography, continued)

Hirakawa maintains an active second career as a jazz pianist. He was educated at Eastman School of Music and in 2006, completed his M.M. degree in jazz studies at New England Conservatory of Music in Boston. He is currently seeking a tenure-track assistant professor position.
Advanced Microscopy Techniques and Ultrafast Lasers: a Symbiotic Development

Speaker: Marco Arrigoni, Coherent, Inc.
Time: Dinner & Networking at 6:00 PM; Presentation at 7:00 PM
Cost: none
Place: National Semiconductor, Auditorium E, 2900 Semiconductor Drive, Santa Clara
Web: www.ewh.ieee.org/r6/scv/leos

After obtaining a Masters Degree in Engineering at Politecnico of Milan, Italy, Marco Arrigoni worked as R&D engineer with Italian defense contractors, developing solid-state laser rangefinders and one of the first European diode-pumped lasers, in 1987. In 1988, he joined Coherent Inc. as R&D Engineer, designing ion lasers systems. In 1995 he moved to international sales and from 1998 to 2000 he managed Coherent's business in Asia, living in Tokyo. After moving back to the United States in 2001, he covered several positions in international marketing and sales. He is currently director of marketing for the scientific market segment. To strike a balance between his technical career and his passion for the old world, he collects roman coins and art, and is fond of classical and jazz music.

Starting with the invention of Multi-Photon Excitation (MPE) Microscopy in 1991, Ultrafast lasers entered biological imaging and research laboratories. The short duration and high peak power of the infrared pulses of light generated by these lasers allowed to image cellular structures and tissues more in depth than any other non-invasive microscopy techniques, and on living (and surviving) animals. In the last decade, other Non-Linear Optics Microscopy techniques using Ultrafast lasers have been developed like Harmonic and CARS Microscopy. Each of these brings its original contribution to providing in-vivo information-rich images of animal and human subjects as well. The development of these novel microscopy techniques is further enabled by each new generation of Ultrafast lasers and, in turn, drives the industry to develop new, dedicated laser sources.
Adaptive Control for Autonomous Underwater Vehicles

Speaker: Conor McGann, Monterey Bay Aquarium Research Institute (MBARI) / Willow Garage

Time: Presentation at 7:00 PM
Cost: none
Place: Carnegie-Mellon West campus, Moffet Field
RSVP: not required
Web: ewh.ieee.org/r6/scv/ras

Conor McGann hails from Dublin, Ireland. He received his Bachelors in Computer Engineering from Trinity College, Dublin in 1990 and his PhD in Computer Science from that same institution in 1995. Subsequently, he co-founded Cunav Technologies, a Dublin based software company which he led as CEO for 3 years. In 1998 Conor married a Texan and emigrated to the US where he joined the supply-chain company, i2 Technologies, and became the Chief Architect for their Customer Management Product Group. In 2002 Conor joined the Planning and Scheduling Group at the NASA Ames Research Center where he led the development of the EUROPA-2 constraint-based temporal planning library which has been used for ground based and onboard planning in a wide range of applications. In November 2006 Conor turned to inner space when he joined the embryonic Autonomous Systems Group of the Monterey Bay Aquarium Research Institute. In May, 2008, Conor returned to the Bay Area to join Willow Garage, a robotics company located in Menlo Park. He continues to collaborate with NASA and MBARI and pursue his interests in autonomous systems.

Autonomous Underwater Vehicles (AUV) are mobile robotic platforms used by the oceanographic community for exploration in diverse environments from the seafloor to the ocean surface. The extensive payload capacity and operational versatility of AUV’s offer a cost-effective alternative to traditional ship-based oceanographic measurements for advancing ocean research. Existing mission control practices rely on manually scripted plans produced prior to mission execution. Mission scripts are prone to error and do not afford adaptability of the vehicle to unanticipated events. Such adaptability is critical to maximize science utility from the limited time, energy and sampling opportunities available for a mission. To address these issues, we have developed and deployed an Adaptive Control System that integrates Planning and Probabilistic State Estimation in a goal-directed hybrid executive, enabling scientists to detect, survey and sample events of an unpredictable nature. The system developed for ocean science is general purpose and adaptable to other ocean going and terrestrial platforms.
This talk discusses the technology platform development for IC design in nano-CMOS technologies. New effects and issues in nano-CMOS are reviewed before the discussion on the contents of the technology platform. Some key components are briefly discussed with the exploration of some further challenges to develop a RF SoC design technology platform. An advanced technology platform with strong links to process and device behavior and efficient simulation approaches is critical to a successful advanced IC design in nano-scale CMOS technologies.

**Biography (continued)**

In 1997, he worked at Cadence Design Systems and then joined Rockwell International. From 1997-2004, he worked at Rockwell Semiconductor Systems, Conexant Systems (a spin-off from Rockwell), and Skyworks Solutions (a spin-off from Conexant), where he was a Principal Engineer, a Manager, and a Senior Manager. Under his leadership the Skyworks technology group was expanded into a strong engineering team that plays a key role in developing Mixed-signal/RF technology for various (ASIC, analog, Mixed-signal, RF) circuit designs. From 2004-2006, he worked in Siliconlinx, Inc., which offers products and services to bridge the gap between IC designers and manufacturing foundries. He is now a full professor in Peking University and the Dean of a newly established research institute of microelectronics in Shanghai.

He has served on many Technical Program Committees and chaired numerous Sub-committees at international conferences, including the IEEE Custom Integrated Circuits Conference (CICC) since 2001 and Radio Frequency Integrated Circuits Symposium since 2002. He organized and participated in numerous workshops and panels related to RFCMOS technology and SoC design. He has authored and co-authored over 90 research papers, two book chapters, two books “MOSFET Modeling & BSIM3 User’s Guide” by Kluwer Academic Publishers (1999), and “Device modeling for analog/RF circuit design” by John Wiley and Sons (2002). He is an IEEE Fellow and an IEEE Distinguished Lecturer of EDS. His research interests include advanced RFCMOS technology, analog/mixed-signal/RF circuit designs for system integration applications.
The Year of Living Dangerously: Extraordinary Results for an Enterprise Agile Revolution and Globalization and Why It Works

Speakers: Steve Greene and Chris Fry; Kevin Walsh
Time: Social at 6:00 PM, Pre-dinner Presentation at 6:30 PM, Dinner at 7:15 PM, Presentation at 7:45 PM
Cost: $25 for IEEE member, $30 non member ($5 more at door)
Place: Ramada Inn, 1217 Wildwood Ave (near 101 and Lawrence Expy), Sunnyvale
RSVP: through the website
Web: www.ieee-scv-ems.org

Chris Fry is a Senior Director at Salesforce.com responsible for platform software development. He specializes in Software as a Service and creating and leading agile teams. He is the author of JSR-173 (Streaming API for XML) and has led the implementation and deployment of massively scalable Web Services at Salesforce.com and BEA. He received his Ph. D. in Cognitive Science from UCSD and was a post-doctoral fellow at UC Berkeley.

Steve Greene is the Director of Tools & Process at Salesforce.com and is responsible for the implementation and evolution of agile methodologies and supporting tools for the Technology organization. He has held numerous senior management positions at On-demand startup and large enterprise software companies including DigitalThink, Hyperion, PeopleSoft/Oracle, SPC and AOL. He brings a wealth of expertise and experience in productivity, process and product delivery. He holds a BS in Computer Engineering from San Jose State University and is a board member of the BayAPLN.

Kevin Walsh is a general partner at Ridge Partners LLC, an investment and buy-out company focused in the high technology sector. He is also the Dean's Executive Professor of Management at the Leavey School of Business and was previously Vice President of Corporate Planning and Worldwide Financial Operations at Sun Microsystems. Prior to joining Sun, Kevin was COO at Spatial Technology and held Vice President positions at Schlumberger and Fairchild Semiconductor in both Europe and the USA. He is a graduate of the London School of Economics, a member of the Institute of Management Consultants and Certified Chartered Accountant (UK).

The Year of Living Dangerously: Extraordinary Results for an Enterprise Agile Revolution

Many software organizations today ask "How do we make an agile transformation and what benefit will we get?" Should you transition your organization to agile all at once or proceed more iteratively, team by team? This talk describes Salesforce.com's year of living dangerously, where we moved our entire R&D organization to an agile model. The key difference in our approach was to throw the switch on 30 teams all at once. Most agile experts thought this was a crazy approach; however, in the end our transition became one of the fastest and largest agile transitions. In just 3 short months we moved our entire team from a waterfall-based approach to an iterative, Scrum based methodology we've named ADM (Adaptive Development Methodology). Over the course of the year we have refined and measured our progress and learned many lessons. This approach was a great risk for the organization that has ultimately delivered dramatic results and extraordinary business value.

Globalization and why it works!

The talk will focus on how Globalization is impacting the world and the US economy and what it means for the future of a skill-based society.
Integrated On-Chip Inductors Using Magnetic Material

Speaker: Don Gardner, Intel Corporation
Time: Cookies & Conversation at 7:30 PM, Presentation at 8:00 PM
Cost: none
Place: Western Digital, 1710 Automation Parkway, San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/mag

Don Gardner has been with Intel Corporation since 1991 and is currently a principal engineer in Intel Research and a visiting scientist at Stanford University. Don received his PhD in Electrical Engineering from Stanford University. He has had appointments as a visiting research scientist at Hitachi Research Labs in Japan and as an instructor at Stanford University. He is the inventor or co-inventor of 56 patents including for inductors using high-frequency magnetic materials, Al-Ti layered metal for interconnections, reflow of copper metal, and embedded ground planes. Don has published and/or presented over 200 electrical engineering, materials science and computer science papers. He has received 3 Best Paper and Poster awards at international conferences and his paper on inductors was judged the best at the IEEE IITC conference. He enjoys bringing new life to old technologies by blending them with different technologies or recent science and new materials. His current interests include magnetic materials for high-frequency inductors, nanostructure design and devices, silicon-based optoelectronic devices, and new process technology.

On-chip inductors with magnetic material are integrated into both advanced 130 nm and 90 nm CMOS processes. The inductors use copper metallization and amorphous CoZrTa magnetic material. Increases in inductance of up to 28× were obtained, significantly greater than prior values for on-chip inductors. With such improvements, the effects of eddy currents, skin effect, and proximity effect become clearly visible at higher frequencies. The CoZrTa was chosen for its good combination of high permeability, good high-temperature stability (>250°C), high saturation magnetization, low magnetostriction, high resistivity, minimal hysteretic loss, and compatibility with silicon technology. The CoZrTa alloy can operate at frequencies up to 9.8 GHz, but tradeoffs exist between frequency, inductance, and quality factor. The effects of increasing the magnetic film thickness on the permeability spectra were measured and modeled. The inductors use magnetic vias and elongated structures to take advantage of the uniaxial magnetic anisotropy. Techniques are presented to extract and examine the effects of magnetic vias on the inductor structures. The inductors with thick copper and thicker magnetic films have inductance densities of up to 1.3 mH/mm², resistances as low as 0.04 W, and quality factors of 8 at 50 MHz.
Thermal Stress Modeling in Electronic and Photonic Engineering: Is FEA the Only Tool?

Speaker: Dr. Ephraim Suhir, CPMT Society Distinguished Lecturer; Bell Laboratories (ret); Dept of Electrical Engineering, UC-Santa Cruz; Dept of Mechanical Engineering, Univ of Maryland

Time: Seated dinner at 6:30 PM, Presentation (no cost) at 7:30 PM

Cost: $25 for dinner

Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, near Lawrence Expy), Sunnyvale

RSVP: by email to Janis Karklins, karklins@ieee.org

Web: www.cpmt.org/scv

Dr. Ephraim Suhir is a Fellow of the IEEE, the American Physical Society (APS), the American Society of Mechanical Engineers (ASME), the Institute of Physics (IoP), UK, and the Society of Plastics Engineers (SPE). He has formed, and is chairing, the IEEE TAB NTDC Group on Portable Information Devices (PIDs), and the IEEE Vehicular Technology Society (VTS) Technical Committee on PIDs, and is co-founder of the ASME Journal of Electronic Packaging and served as its Technical Editor (Editor-in-Chief) for eight years (1993-2001). Ephraim holds 20 US patents and has authored about 300 technical publications (papers, book chapters, books). He is currently a BoG Member and Distinguished Lecturer of the IEEE CPMT Society and is Associate Editor of the IEEE CPMT Transactions on Advanced Packaging. He has organized many successful conferences and symposia in the USA, Europe and Asia, and presented numerous keynote and invited talks worldwide.

Some major awards: 2004 ASME Worcester Read Warner Medal for outstanding contributions to the permanent literature of engineering through a series of papers in Mechanical, Microelectronic, and Optoelectronic Engineering, which established a new discipline known as the Structural Analysis of Microelectronic and Photonic Systems; (cont.)

This talk addresses the role and attributes of, as well as the state-of-the art and major findings in, the field of analytical thermal stress modeling in electronic and photonic engineering. The emphasis is on simple and practical models that can be and have been used in the physical design and reliability evaluations of electronic and photonic assemblies, structures and packages.

It covers the role, attributes, merits and shortcomings of analytical thermal stress modeling, and its interaction with numerical (primarily finite-element) and experimental techniques. The topics addressed include Timoshenko’s bi-metal thermostat theory and its extension; thermally matched assemblies and assemblies bonded at the ends; design recommendations; thin film structures; polymeric materials and plastic packages of IC devices; photonic (primarily fiber optic) structures; and application of probabilistic approaches. Thermal stress modeling in nano-materials and nano-structures is also briefly discussed.

A review paper "Analytical Thermal Stress Modeling in Electronic and Photonic Systems" is available upon request. It will be published later on this year in the ASME Applied Mechanics Reviews.

Biography (continued)

… 2001 IMAPS John A. Wagnon Technical Achievement Award for outstanding contributions to the technical knowledge of the microelectronics, optoelectronics, and packaging industry; 2000 IEEE-CPMT Outstanding Sustained Technical Contribution Award for outstanding, sustained and continuing contributions to the technologies in fields encompassed by the CPMT Society; 2000 SPE International Engineering/Technology (Fred O. Conley) Award for outstanding pioneering and continuing contributions to plastics engineering; 1999 ASME and Pi-Tau-Sigma Charles Russ Richards Memorial Award for outstanding contributions to mechanical engineering, and 1996 Bell Laboratories Distinguished Member of Technical Staff Award for developing extremely accurate and robust engineering mechanics methods for predicting the reliability, performance, and mechanical behavior of complex structures used in manufacturing Lucent Technologies products.
The IEEE PACE will have the honor of having George Hanover, 2007 IEEE-USA Congressional Fellow. He addressed innovation and competitiveness issues as a staffer for the Environment, Technology and Standards Subcommittee of the House Science Committee. George also served on the personal staff of Rep. Dana Rohrabacher (R-Calif.), a member of the House Science Committee. George will discuss an Engineer’s perspective on the "Government Process" and the IEEE-USA's involvement in that process.

If you’ve wondered how the legislative process works in Washington, and how IEEE-USA is influencing it, then put this meeting on your calendar.

We will also be having a Senior member Upgrade Information session prior to the talk. If you’ve been putting off applying for Senior member grade, then bring your resume and we’ll get you going – painlessly!

Congressional Insights and Senior Member Upgrade Information Session

Speaker: George Hanover, 2007 IEEE-USA Congressional Fellow
Time: Dinner and networking 6:00 PM, Senior Member Upgrade Information session at 6:45 PM, Presentation 7:00 PM
Cost: none (food, beverages can be purchased on-site)
Place: Grand Indian Buffet, 1214 Apollo Way, Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/PACE
Past, Present and Future of Solar Thermal Generation

Speaker: Bruce Kelly, P.E.
Time: Lunch and Presentation at Noon
Cost: Free for IEEE members, $5 for non-members
Place: Pacific Gas & Electric Office, 77 Beale St. Room 305, San Francisco
RSVP: by email to Anupama Pandey, apandey@nexant.com, 415-369-1096
Web: www.e-grid.net/docs/0806-sf-pes.pdf

Mr. Bruce Kelly has 30 years of experience in design, engineering, and economic assessment of advanced renewable energy conversion systems and is a renowned expert in the area of solar thermal technologies. He has been responsible for the conceptual, preliminary, and final design and economic analysis of advanced solar thermal energy systems, emissions systems for fossil-fired distributed generators, and hydrogen delivery infrastructures.

Mr. Kelly holds a B.S. in Mechanical Engineering from the University of California, Berkeley, 1973 and a M.S. in Mechanical Engineering University of California, Berkeley, 1976. He is a registered mechanical engineer in California and a member of Tau Beta Pi. He has co-authored several papers on solar thermal energy and is co-holder of a patent on an air-cooled central receiver concept.

In response to the energy crisis of the early 1970’s, the US Department of Energy initiated a range of R&D activities in central receiver, parabolic trough, and dish Stirling solar thermal technologies. The most ambitious of the DOE activities was the 10 MWe, $150 million Solar One central receiver power plant near Barstow, California. Powerful tax incentives in the 1980’s led to the private financing and construction of 9 parabolic trough projects in the California Mojave Desert. In the 1990’s, the DOE and several Southwest utilities cooperatively financed a retrofit of the Solar One central receiver project to an advanced, nitrate salt technology.

Today, several privately-financed parabolic trough projects are under development, driven by a favorable combination of a 30 percent investment tax credit and utility renewable portfolio standards.

In the future, technical developments could include large (>100 MWe) nitrate salt central receiver power plants, and the use of inorganic coolants in parabolic trough collector fields.
MobileTV/Video Workshop

Speakers: Christopher Dow, Director of Software, Macrovision; and others (Co-Sponsored by NATEA)

Time: 6:00 - 9:00 PM
Cost: none
Place: National Semiconductor, Building E, Conference Room, 2900 Semiconductor Dr, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/comsoc

More details will be available on the website.
Hybrid Organic-Inorganic Devices Using Self-Assembly Techniques: Application To Solar Cells

Speaker: Dr. Geetha R Dholakia, Senior Research Scientist, Advanced Aerospace and Materials Group, NASA Ames Research Center

Time: Registration & light lunch at 11:30 AM; Presentation at Noon

Cost: IEEE Members and Students $5, Non-Members $10

Place: National Semiconductor Bldg E-1 CMA Room, 2900 Semiconductor Drive, Santa Clara

RSVP: on our website

Web: www.ieee.org/nano

In recent years there has been a tremendous amount of research directed towards the development of low dimensional nanostructured materials having a broad range of physical and electronic properties. Assembly of nanoscale objects, both for routine transport measurements as well as for integration into functional devices requires new techniques to efficiently manipulate them at the nanoscale. Self-assembly is a promising technique for manipulating and assembling nanoscale structures. This talk will focus on self-assembly of molecular monolayers and multilayers. The critical role played by orientation, order and nanostructure in the electronic transport properties and the device performance will be discussed. Finally, possibilities in the synthesis of oxide nanowires and their applications in hybrid organic solar cells will be discussed.

Geetha Dholakia is a Senior Research Scientist at the Advanced Aerospace and Materials Devices group, NASA Ames Research Center. At NASA, she works in the areas of soft condensed matter, multifunctional materials synthesis and electronic transport measurements in nanomaterials. She conducts research at the interface of Physics, Materials Science and Chemistry. She has developed scanning probe instruments and is currently also involved in instrument development for NASA on board planetary missions. She received a Ph.D in Physics from the Indian Institute of Science, Bangalore India and a Masters in Physics from the Indian Institute of Technology, Madras, India. She also held a Visiting Scientist position in the Applied Physics Department at Rensselaer Polytechnic Institute, Troy NY, prior to her current position at NASA Ames.
When Location Becomes a Utility:

2007 was the year when “GPS” became a household word like Kleenex or Xerox. Location determination capability is on its way to becoming “table stakes”, i.e., a basic feature that is part of mobile devices, and no longer just for regulatory reasons. The speaker will first introduce Rosum’s use of broadcast TV signals for location determination, and then will explore what applications become possible when location awareness becomes an always-available utility.

Locations: Because Life Moves

I will overview SiRF and location-aware devices then cover recent LBS market trends, an overview of various location technologies, an example LBS system architecture and end with SiRF’s wireless solutions portfolio as it maps to the LBS market.

Jon Metzler is Strategic Initiatives and Government Affairs Director for Rosum Corporation. He is responsible for partnership development in mobile TV markets, standards development, and regulatory advocacy on public safety and broadcast TV issues. Prior to joining Rosum, Jon was Vice President at Performance Analysis Inc, a services firm specializing in business development in Asia for technology companies. Prior to joining PAI, Jon was part of multiple successful launches into the Japanese market, in the fields of technology, services and media. Jon is a graduate of the MBA/MA-Asian Studies program at UC-Berkeley. He is now an advisor to the UC-Berkeley Management of Technology program. Jon also has a B.A. from the University of Michigan. Jon publishes regularly on technology and policy issues and is a member of the E911 Institute.

Dave Reid is Director of Business Development, SiRF Technology Inc. and is in charge of global business development for the company’s wireless segment. In this role, Reid is responsible for identifying and developing new business prospects for SiRF’s wireless solutions, which include GPS chipsets and carrier-grade software for use in handsets, smartphones, personal locators, asset tracking devices, fleet management systems and carrier infrastructure globally for location-based services (LBS) and mobile resource management (MRM). Reid also develops new opportunities for the SiRFecosystem, a comprehensive suite of products and services designed to help the global LBS developer community more easily develop, test, and market their location applications. (Cont.)
WiMedia Ultra-Wide-Band Communication

Speaker: Domine M. W. Leenaerts, NXP Semiconductors
Time: Refreshments at 6:00 PM; Presentation at 6:30 PM
Cost: small donation for food
Place: National Semiconductor Building E, Auditorium, 2900 Semiconductor Dr., Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/ssc

Since the FCC opened up the spectrum for Ultra Wide Band (UWB) operation in the 3.1 to 10.6GHz range, several standards have been proposed to realize moderate and high rate short-range communication systems. Under the WiMedia umbrella, industry incorporated UWB as the technology to achieve high data rates up to 480Mbps for the wireless USB 2.0 applications. The WiMedia standard uses multi-band DCM/QPSK-OFDM modulated sub-bands of 528 MHz. A fast frequency-hopping scheme is applied to achieve efficient and robust communication links up to 10m distance. As the standard will be adopted by the cellular market, co-existence with other communication standards as GSM/WCDMA and WLAN/BT/GPS is an important but challenging system requirement.

Philips/NXP Semiconductors, Research is active in this field from the beginning of 2003. The presentation will give an overview how the UWB standard evolved and how the interesting research challenges were tackled (at least within Philips/NXP). In the early days the transceiver designs were developed in (SiGe) BiCMOS technologies with the focus on operation in band group 1 only, i.e. the frequency band from 3432MHz to 4488MHz. Later, the focus shifted towards CMOS designs targeting not only band group 1 but also band group 3 (6600MHz – 7656MHz) and even band group 6 (7656MHz – 8712MHz). Some insights in circuit design and measured performance will be provided during this presentation.

Domine M. W. Leenaerts received the Ph.D. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, the Netherlands, in 1992. From 1992 to 1999, he was with Eindhoven University of Technology as an Associate Professor with the Micro-electronic Circuit Design group. In 1995, he was a Visiting Scholar with the Department of Electrical Engineering and Computer Science, University of California, Berkeley. In 1997, he was an Invited Professor at Ecole Polytechnique Federale de Lausanne, Switzerland. From 1999 to 2006 he was a Principal Scientist with Philips Research Laboratories, Eindhoven, where he was involved in RF integrated transceiver design. In 2006, he moved to NXP Semiconductors, Research as Senior Principal Scientist in RF IC design.

He has published over 150 papers in scientific and technical journals and conference proceedings. He holds several US patents. He has coauthored several books, including Circuit Design for RF Transceivers (Boston, MA: Kluwer, 2001). Dr. Leenaerts served as an IEEE Distinguished Lecturer in 2001-2003 and served as Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-PART I (2002-2004) and is since 2007 Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is the IEEE Circuits and Systems Society Member representative to the IEEE Solid-State Circuits Society Administrative Committee since 2006. Dr. Leenaerts serves currently on the Technical Program Committee of the European Solid-State Circuits Conference (ESSCIRC), the IEEE Radio Frequency Integrated Circuits (RFIC), and IEEE International Solid-State Circuits Conference (ISSCC). Dr. Leenaerts is Fellow IEEE.
Power system grounding is considered the backbone of any electrical distribution system. IEEE standard 141 (IEEE Recommended Practice for Grounding of Industrial and Commercial Power Systems) clearly demonstrates the various power system grounding methods and their associated characteristics. This presentation will review the following subjects as they relate to IEEE standards:

- Solidly and effectively grounded systems
- Ungrounded and high resistance grounded systems
- Field Measurements on an ungrounded system during a ground fault
- Low Resistance Grounded Systems

The presentation will also introduce the modern concept of the Hybrid High Resistance Grounding Systems (HHRG) and its applications as it relates to transformers, motors and generators.

**Rakan El-Mahayni** is currently working with Eaton Corporation in Livermore as a Team Leader for the Power System Engineering (PSE) Division in the Northwest. The PSE division provides power system studies such as short circuit, coordination, arc flash, grounding and harmonic analyses for electrical power distribution systems.

In 1998, after graduating from University of Damascus, Syria from the Electrical Power Engineering Division, he joined Siemens AG as a Testing and Commissioning Engineer for the 400 KV power interconnection projects between the Middle East and Europe. In 2002 he joined Eaton Corporation as a Field Service Engineer conducting start up, testing and maintenance for medium and low voltage systems. In 2006, he graduated from California State University, Sacramento with a Masters Degree in Electrical Power Engineering.
Sustainability - What It Means to Product Safety Engineers and Why They Should Care

Speaker: Sanjay Baliga, Environmental Health & Safety (EHS) Division, SEMI (Semiconductor Equipment and Materials International)

Time: 5:45 PM dinner at El Torito Mexican Restaurant; 7:00 PM presentation at Applied Materials Bowers Cafe

Cost: Dinner is no-host; no cost for presentation

Place: El Torito Mexican Restaurant, 2950 Lakeside Drive, Santa Clara; Applied Materials, Bowers Cafe, 3090 Bowers Ave, Santa Clara

RSVP: not required

Web: www.ewh.ieee.org/r6/scv/pses

Unless you've been asleep for the past year, you're probably aware of the intense global focus on sustainability. For everything from renewable energy to global warming, sustainability is the theme of the day. But is it just a buzz word that will be gone next year, replaced with something new? Or should we really take notice?

This presentation will help to define and explain sustainability, including why it's important to the world, to business, and to the product safety engineer.

Sanjay Baliga currently is a Senior Manager in the Environmental Health & Safety (EHS) Division of SEMI (Semiconductor Equipment and Materials International) in San Jose. He is responsible for many EHS and sustainability activities at SEMI, such as co-coordinating the Global Care program, providing regulatory and compliance assistance to member companies, supporting the EHS International Compliance and Regulatory Committee (ICRC) and running other SEMI regional office programs.

Before coming to SEMI, Baliga was an independent consultant providing regulatory, scientific, and technical consulting services to a wide variety of chemical industry companies, trade associations and research councils. He has more than 15 years of professional experience addressing issues at the interface of science, engineering, management and policy, using his expertise in environmental risk management and sustainability.

Baliga has degrees from schools in Palo Alto, Ann Arbor and New Haven.
Cloud Computing denotes the latest trend in application development for Internet services, relying on clouds of servers to handle tasks that used to be managed by individual machines. With Cloud Computing, developers take important services, such as email, calendars, and word processing, and host them entirely online, powered by a vast array (or cloud) of interdependent commodity servers. Cloud Computing presents advantages for organizations seeking to centralize the management of software and data storage, with guarantees on reliability and security for their users. Recently, we have seen many efforts of the commercialization of the cloud, such as Amazon's EC2/S3/SimpleDB, Google's App Engine, Microsoft's SQL Server data services and IBM's "Blue Cloud" service. At the same time, open source projects such as Hadoop and ZooKeeper offer various software components that are essential for building a cloud infrastructure.

We hope to bring together eminent researchers and practitioners from key research labs, companies, and open source communities to give us a quick overview of cloud computing. In addition, these speakers will present their views on the opportunities and challenges of cloud computing, either from technology aspect or business aspect.

This joint IEEE-NATEA conference on an emerging technology is aimed to provide IEEE and NATEA members with an inexpensive solid overview of a technology that may affect their work and careers in the near future. This annual conference series have been traditionally held at Stanford University on a Saturday. This year the date is July 19th at the Braun Auditorium. Over the past 9 years we have covered such topics as RFID, SOC, Bioinformatics, Nanotechnology, and multicore.