

CHAPTER MEETINGS

- SCV-TMC - 1/7 | **Value-based Scheduling: Get your Organization's Priorities Straight** - multiple projects, shifting priorities,... [\[more\]](#)
- EnCorps - 1/10 | **Open House: Transitioning for Engineering Professionals** - switching from engineering to high-school teaching ... [\[more\]](#)
- SCV-Mag - 1/12 | **A New Paradigm for Exchange Bias in Polycrystalline Films** - granular model, thermal and magnetic cycling, [\[more\]](#)
- SCV-CPMT - 1/13 | **High-Reliability Through-Silicon Via (TSV) Solutions for Image Sensor Packaging** - module trends, barriers... [\[more\]](#)
- SCV-ComSoc - 1/13 | **The Smart Packet Core for 3G and 4G Mobile Networks** - Radio Access Network (RAN), IP backbone routers ... [\[more\]](#)
- SCV-Nano - 1/19 | **Nanotechnology in 2010 and Beyond: Beating the Recession, Launching Big Ideas** - alignment with research labss ... [\[more\]](#)
- SCV-CNSV - 1/19 | **What Everyone Should Know About China** - doing business, cultural perspectives, executive interviews ... [\[more\]](#)
- SCV-EMB - 1/20 | **SMRT (Single-Molecule, Real-Time) Biology** - single-molecule resolution, dynamics, commercial application ... [\[more\]](#)
- SCV-SSC - 1/21 | **Integrated Circuit Design with Nano-Electro-Mechanical Switches** - circuit architectures, energy, performance ... [\[more\]](#)
- SCV-CSS - 1/21 | **Robot Team Coordination and Simultaneous Localization and Mapping (SLAM)** - control, 2D laser, applications ... [\[more\]](#)
- SCV-AP - 1/21 | **Channel Surfing: Managing Propagation in Broad-band Wireless Systems** - WiMAX, LTE, OFDMA modulation ... [\[more\]](#)
- SCV-CNSV - 1/22 | **Patents for Engineering Consultants: The Basics, Your Opportunities, and Your Risks** - infringement, licensing ... [\[more\]](#)
- SF-IAS - 1/26 | **Cogeneration: An Electrical Perspective** - design approach, interconnection to grid, distributed generation ... [\[more\]](#)
- SCV-PSES - 1/26 | **Codes, Standards and Listings: Who Requires What, and Why** - resources, agencies, sustainability standards ... [\[more\]](#)
- OEB-Mag - 1/27 | **Non-adiabatic Spin-torques in Narrow Magnetic Domain Walls** - magnitude, spin-dependent transport, dynamics ... [\[more\]](#)
- IEEE-USA - 1/28 | **There's No Crying in Business: How Women Can Succeed in Male-Dominated Industries** - gender barriers, tools... [\[more\]](#)
- SCV-CPMT - 1/28 | **This is In: Thinning of IC Chips** - flawless silicon crystal, singulation, vertical stacking, assembly, packaging ... [\[more\]](#)
- SCV-EDS - 1/29 | **3D Interconnect: Shaping Future Technology** - higher densities, smaller form factors, greater functionality ... [\[more\]](#)
- SCV-CPMT - 2/10 | **Large-Scale Print Manufacturing of Complex, Miniature 3D Structures** - chambers, channels, sensors, circuits ... [\[more\]](#)
- SCV-Mag - 2/16 | **Technology Trends for Magnetic Storage: What Is The Future?** - miniaturization, multiterabyte, advanced heads, alternative technologies ... [\[more\]](#)
- SCV-EMB - 2/17 | **Optical Coherence Tomography – From Bench to Bedside** - cross-sectional images, ophthalmology, retinal diseases ... [\[more\]](#)
- SF-IAS - 2/23 | **Getting the Most Out of Your Electrical Room** - work clearance, Equipment sizing, utility requirements, seismic ... [\[more\]](#)

Conference Calendar

- Jan 25-28: **Annual Reliability and Maintainability Symposium** - Doubletree Hotel, San Jose [\[more\]](#)
- Feb 21-25: **Semiconductor Thermal Modeling, Measurement and Management Symposium (SEMI-THERM)** Santa Clara Convention Center [\[more\]](#)
- February 23-25: **Ethernet Technology Summit** -- Wyndham Hotel, San Jose [\[more\]](#)
- March 22-24: **Int'l Symposium on Quality Electronic Design (ISQED)** DoubleTree Hotel, San Jose [\[more\]](#)
- April 12-16: **Asia-Pacific Symposium on Electromagnetic Compatibility** - Beijing, China [\[more\]](#)

Career Assistance

- Professional Skills Courses** [\[more\]](#)
- Managing Time & Multiple Priorities
 - Project Mgmt
 - Virtual Teams: Working Together Apart
 - Management Essentials
 - Presentation Skills for Engineers *and more*

Technical Classes at UC-SC Extension [\[more\]](#)

- Embedded Systems and VLSI Engineering Program
- Overview - Software Development Program Overview - Network Engineering and System Security Program
- Overview ... and more

Santa Clara Univ, Grad School of Engineering

- CMOS Technology, Sustainable IT** [\[more\]](#)
- 5- one-day seminars

1-day class in S.F.

Photovoltaics Technology and Manufacturing

3-, 4-day classes in S.J.

CDMA and EV-DO Technology Semiconductor Reliability Failure and Yield Analysis

[\[more\]](#)

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page 3

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IEEE GRID is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for news for technologists, managers and professors, the editorial objectives of IEEE GRID are to inform readers of newsworthy IEEE activities sponsored by local IEEE units (Chapters, Affinity Groups) taking place in and around the Bay Area; to publicize locally sponsored conferences and seminars; to publish paid advertising for conferences, workshops, symposia and classes coming to the Bay Area; and advertise services provided by local firms and entrepreneurs.

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From the Editor ...

As we begin a new year, it's a good time to reflect on goals for our professional lives. For the 95% of our members who are fully employed, it's appropriate to think about the next steps in gaining experience and/or new knowledge – so you can continue on an upward path in your career. It's more important than ever to “network” with others in your field, such as at IEEE chapter meetings, to keep aware of new developments – of who's doing what in our industry, who you'd like to know, who might be of help in the future – remember, they're doing the same thing. You should also shoot for taking an “update” course each year, and probably attending at least one conference in your discipline.

And yes, if you're currently a “Member in Transition” and are looking for a new position, networking at local meetings and events is more important than ever. Many of you have joined our SF Bay LinkedIn Group, to share ideas, look through our posted jobs in the Bay Area, and learn more about improving your own LinkedIn web page – as you've likely heard, about 2/3rds of jobs aren't publicized, but are discovered and taken through services like LinkedIn. Polish your “elevator speech,” and then reach out and talk to others in your field to see if any of them know of potential openings that would fit your skills, or of companies that might be hiring.

The local IEEE wants to help you to succeed in your career. Getting involved is the first step for tapping this assistance. Talk to the new officers for our local chapters of interest to you, to see how you might participate. Find them through the GRID website!

Paul

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: www.e-GRID.net



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Embedded Systems and VLSI Engineering Program Overview (20544 - free) on January 11

Software Development Program Overview (3085 - free) on January 12

Network Engineering and System Security Program Overview (20545 - free) on January 13

Renewable Energy (22410) starts on January 21

SystemVerilog for Advanced Design Verification (18966) starts on January 25

Logic Synthesis, Introduction (4377) starts on January 25

Real-Time Embedded Systems Architecture and Programming (5381) starts on January 26

Design Simulation with Verilog and SystemVerilog (6932) starts on January 26

To view the full fall catalog, visit

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Northern CA First Lego League needs volunteer judges for this year's robotics tournaments. No experience required, just a short training class and a conference call. We need your volunteering help for these budding engineers, mathematicians and scientists. We need 180 judges, referees and other positions to help at tournaments all over the Valley. The tournaments will be held on Saturdays and a few Sundays.

Please sign up at :

www.playingatlearning.org/FLL/volunteer.html#specialtyrole
and send an email to flvolunteer@playingatlearning.org
to let them know ASAP.

Submitted by Lee Colby, K-12 Coordinator, SCV Section

PACE Network
Santa Clara Valley Section, IEEE

**Unemployed? Join our
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Finding a new job is hard -- let the SCV Section's **PACE Task Force** give you a hand. Limited to current IEEE Members throughout the Bay Area, we're committed to using the brain-power of our talented members to help you develop a strong LinkedIn page (since that's where recruiters look), find opportunities on our Jobs Board, and learn from our Discussion Board. November is our start-up time, but you'll find more assistance there as the year comes to a close.

Request to be included, at

www.linkedin.com/groups?gid=2403879

(yes, you'll need a LinkedIn account –
but you've already created one, right?)

Paul Wesling

Call for Participation

ISQED 2010, 11th International Symposium on

QUALITY ELECTRONIC DESIGN

March 22-24, 2010

DoubleTree Hotel, San Jose, CA, USA



www.isqed.org



The International Symposium on Quality Electronic Design (ISQED) is a leading Electronic Design & Design Automation conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading international conference dealing with design for manufacturability and quality issues front-to-back. ISQED emphasizes a holistic approach toward electronic design and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting over 130 technical presentations, six keynote speakers, panel discussions, workshops/tutorials and other informal meetings.

CONFERENCE HIGHLIGHTS

TUTORIALS/WORKSHOPS

ISQED2010 is pleased to offer a single full-day tutorial track, as well as several embedded tutorials. These tutorials explore critical areas in electronic design and are presented by several experts in their respective fields. List of topics covered is as follows:

Beyond 32 nm Technology

K. Maitra - Global Foundries

Energy Efficient Digital Circuit Design

Benton Calhoun - University of Virginia

Alternate Memories

Stuart Parkin - IBM

SOC Verification

Ken Albin - AMD

Paving the Road for 3D TSV Design

Pol Marchal - IMEC

Microprocessor Architecture Impacts on Power

Dave Ayers - Intel

A Scalable Methodology for Analog & Mixed-Signal Verification

(Embedded Tutorial)

Shyam Rapaka, Tapan Halder - Synopsys

Field Solver Solutions for IC level design

(Embedded Tutorial)

Maxim Ershov, Silicon Frontline

Field Solver Solutions for System Level & RF

(Embedded Tutorial)

Dipanjn Gope, Swagato Chakraborty - Physware

Vikram Jandhyala - University of Washington, Seattle

KEYNOTES

Plenary sessions will be held on Tuesday and Wednesday mornings. Several industry leaders will discuss the issues surrounding electronic design, design for yield and manufacturability and other critical topics from various point of views. Preliminary list of keynote speakers includes:

Henry Juskiewicz, CEO - Gibson Guitars

Jim Elliott, Vice President of Memory Marketing - Samsung Semiconductor

Aki Fujimura, CEO - D2S & eBeam Initaitave

Antun Domic, Senior Vice President and General Manager - Synopsys

Shankar Krishnamoorthy, Senior Vice President and VP - Mentor Graphics

Steve Glaser, Corporate VP, Cadence

Mark Gogolewski, CTO, Denali

LUNCHEON KEYNOTE

The Test of the Future: Some Thoughts for the Next Decade

Antun Domic, Senior VP and GM - Synopsys

PANEL DISCUSSIONS

The topic of panel discussion on Tuesday evening is as follows:

1. Long Life Cycle Design - Is It Really Different from Traditional CE?

Moderator: **Tets Maniwa**

ISQED Awards

ISQED Quality Award (IQ-Award) ceremony will be held during Tuesday March 23 luncheon. Best papers will be also announced during the same session.

VENDOR EXHIBITION

ISQED2010 Exhibition floor will be open on Tuesday afternoon, March 22, and features vendors offering design tools, methodologies, and services in the areas of design for manufacturing, yield, reliability, and quality. Exhibition includes embedded tutorials, panel discussions, and over 40 technical presentations. Exhibition floor attendance is free but needs advance on-line registration.

TECHNICAL SESSIONS

ISQED Technical sessions start on Tuesday March 23, and continue until the afternoon of Wednesday, March 24. Beside the above plenary sessions, panel discussions, and workshops, the program consists of over 20 technical sessions featuring near 150 papers on various challenging topics related to design for manufacturability and quality. A partial list of topics is shown below. Detail program would be available on the web at www.isqed.org.

- ❖ EDA Methodologies, Tools, Flows & IP Cores; Interoperability and Reuse
- ❖ Design for Manufacturability & Quality
- ❖ Design Verification and Design for Testability
- ❖ Package - IC Design Interactions & Co-Design
- ❖ Design of Reliable Circuits and Systems

- ❖ Power-conscious Devices, Interconnects, and Circuits
- ❖ Physical Design, Methodologies & Tools
- ❖ Emerging/Innovative Process & Device Technologies
- ❖ System Level Design, Methodologies and Tools (SDM)

REGISTRATION

Please refer to ISQED web site at www.isqed.org for information regarding the tutorials, conference, and hotel registration. Direct all conference inquiries to isqed2010@isqed.org. Early registration is recommended to take advantage of the discounted registration fee.

IEEE Professional Skills Courses

Managing Time & Multiple Priorities

- Date/Time: Wednesday, Jan 13, 8:30AM-12:30PM
- Location: Brocade Communication, Santa Clara
- Fee: \$300 for IEEE Members; \$350 non-members

"I enjoyed this class very much. I thought it was very informative and useful. It really made me more aware of how I can organize my time."

Virtual Teams: Working Together Apart

- Date/Time: Thursday, Jan 14, 9:00AM – 5:00PM
- Location: – Synopsys, Mountain View
- Fee: \$400 for IEEE Members; \$500 non-members

Learn how to turn the liabilities of long-distance communication into powerful assets for the planning and execution of complex projects when contributors must coordinate their efforts in the face of time, distance and cultural barriers. Study best practices in project planning and collaboration, remote meeting management, and effective communication to create a coherent picture of how to get things done in today's highly distributed team environments.

SCV Chapters, Technology Management & Components, Packaging and Manufacturing Technology Societies

Project Management: Team-Based Accountability

- Date/Time: Tues/Wed, Feb 16-17, 9 AM – 5 PM
- Location: – TIBCO Software, Palo Alto
- Fee: \$625 for IEEE Members; \$700 non-members

Management Essentials

- Date/Time: Tues/Wed, March 16-17, 9 AM – 5 PM
- Location: – TIBCO Software, Palo Alto
- Fee: \$625 for IEEE Members; \$700 non-members

"Thank you!! I wish I could have had this knowledge along time ago when I first became a supervisor."

-Sales Operations Supervisor, @Road

Presentation Skills for Engineers

- Date/Time: Wed, March 17, 9 AM – 5 PM
- Location: – Integrated Device Technology, SJ
- Fee: \$500 for IEEE Members; \$550 non-members

For complete course information, schedule, and registration form, see our website:

www.EffectiveTraining.com

SEMI-THERM® 26

IEEE TWENTY-SIXTH ANNUAL

Semiconductor Thermal Measurement, Modeling and Management Symposium and Exposition

February 21-25, 2010 Hyatt Regency Santa Clara Convention Center

The twenty-sixth annual SEMI-THERM Symposium is an international forum dedicated to the thermal design and characterization of electronic components and systems. The symposium fosters the exchange of knowledge between practitioners and leading experts from industry and academia from around the world.

SHORT COURSES (Sunday and Monday)

Design of Air and Water Cooled Heat Exchangers for Electronics Cooling, Prof. Al Ortega, Villanova

Cooling Challenges in 3D Packaging, Prof. Dereje Agonafer, University of Texas at Arlington

Estimating Experimental Uncertainty, Robert J. Moffat, Ph.D., Stanford University (Emeritus)

Energy Efficient Thermal Management of Data Centers, Prof. Yogendra Joshi, Georgia Tech

Evening Tutorial: "Thermal Measurements, Facts and Artifacts", Gabor Farkas, Mentor Graphics MicReD Division

SESSIONS

- Modeling & Simulation I & II
- Thermal Issues in 3D Packaging
- Micro-Scale Cooling
- Materials
- Green Technologies
- Experimental Methods I & II
- Thermal Issues in Multicore Architectures
- Single and Two-Phase Cooling
- LED Thermal Measurement
- Posters
- Embedded Tutorial
- Special Event: Academic Research Capability

EXHIBITS AND VENDOR WORKSHOPS

Afternoons, Tuesday and Wednesday, February 23, 24
Complimentary Exhibits Admission and Wednesday reception

Register On-line: (save, through January 15!)

www.semi-therm.org

For further information about exhibiting:
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Photovoltaics Technology and Manufacturing

February 1, 2010

Regus Business Center, 71 Stevenson St, S.F.

Solar energy is again being seriously considered for widespread implementation. Since the 1970s, a number of breakthroughs in photovoltaic technology have made electricity generation from light more feasible and economical. Today, many companies are now developing and introducing technologies to harness power from the sun.

This one-day course goes in depth to describe semiconductor photovoltaic technology and manufacturing. It is designed for every manager, engineer, and technician entering the photovoltaic field, whether it be working directly for a photovoltaic manufacturer or system integrator or selling to PV manufacturers.

The course covers seven major topic areas:

- Characteristics of Solar Radiation
- Semiconductor Material Properties
- Junction Properties
- Efficiency and Losses
- Design of Silicon Cells
- High Efficiency Designs
- Silicon Solar Cell Fabrication

CDMA and EV-DO Technology

February 8-10, 2010

Regus Business Center, 2033 Gateway Place, S.J.

Code Division Multiple Access (CDMA) is an increasingly popular method for handling higher volumes of calls. This spread-spectrum technique is resistant to interference and jamming, provides for more calls to be made on a single frequency, allows for frequency reuse, and permits soft handoffs. Evolution Data Optimized (EV-DO) is designed as an evolution of the CDMA 2000 standard that supports higher bandwidths, enabling a wider range of wireless data services. Both the CDMA and EV-DO standards require an in-depth understanding for engineers to correctly and efficiently implement them. This 3-day CDMA and EV-DO Technology course offers an in-depth look into the technology, standard, algorithms, and issues associated with the two wireless standards. We emphasize the basics surrounding each standard and delve into the current issues related to manufacturing next-generation devices.

By focusing on the basics of the technologies and the issues surrounding them, participants will learn how to optimize performance and efficiently implement the standards in a wireless network. Our instructors work hard to explain the standards without delving heavily into the complex computer science algorithms that normally accompany this discipline.

Semiconductor Reliability

February 8-10, 2010

Regus Business Center, 2033 Gateway Place, S.J.

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing, and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve trade-offs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. Analysis and experimentation is now performed at the wafer level instead of the packaging level. This requires knowledge of experiment design, testing, technology, processing, materials science, chemistry, and customer expectations. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate.

This 3-day course offers detailed instruction on a variety of subjects pertaining to semiconductor reliability. It is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, using semiconductor components, or supplying tools to the industry. Learn how to determine the failure mechanisms that might occur, test for them, develop models for them, and eliminate them from the product.

Failure and Yield Analysis

February 15-18, 2010

Regus Business Center, 2033 Gateway Place, S.J.

Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day.

This 4-day course offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. By focusing on a *Do It Right the First Time* approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

For more information, or to register for the courses, please visit our website:

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February 24-25, 2010 • Wyndham Hotel, San Jose

Ethernet Everywhere!

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10 GbE: Current Status and Future Trends

Ethernet: An Energy-Efficient Technology

Power Over Ethernet

Ethernet Technology Summit focuses on the use of Ethernet throughout the networking space. Attend this event and increase your knowledge of High-speed Ethernet, Ethernet backbones, quality-of-service, management tools, low-power Ethernet, power-over-Ethernet, data center applications, telecom applications, Ethernet security, terabit Ethernet and much more!

Topics of Interest

- 10-Gigabit Ethernet
- 40/100-Gigabit Ethernet
- Carrier Ethernet
- Backbone applications
- Low-power Ethernet
- Quality of service issues
- Power-over-Ethernet
- Software
- Ethernet chips
- Test equipment
- Ethernet processors
- Security
- Storage applications (FCoE)
- Consumer/home applications

“By 2011–2012, the majority of access and aggregation equipment being deployed by carriers around the world will be IP, Ethernet, and WDM, not SONET/SDH. In 2007 and especially in 2008, we’re seeing more carriers using Ethernet, and more carriers conducting interoperability tests of all sorts of Ethernet products for residential broadband, business connections, and mobile backhaul.”

- Michael Howard, Infonetics Research, May 2008

Get the latest information from the experts who are creating the standards, developing the state-of-the-art chips and adapters, heading the major trade organizations, and extending Ethernet into new applications in WANs, storage, wireless, home, and backbones. Includes customer reactions and the latest market research. Keynotes from Ethernet Alliance and MEF (Metro Ethernet Forum).

Who Should Attend?

- Design, software, and test engineers
- Communications specialists
- Hardware and software designers
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- Systems analysts and engineers
- High-performance computing specialists
- Embedded systems designers
- Applications engineers
- Engineering managers
- Solution providers and consultants
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RAMS[®] *The Annual Reliability and Maintainability Symposium*

Transcending Traditional Reliability Approaches – From Theory to Practice

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RAMS is a yearly gathering of the product assurance disciplines where training, tutorials, and the latest technical practices, procedures, and results are presented in easy-to-utilize forums. Now in our 56th consecutive year, RAMS has consistently provided value for the “ilities” through published papers, informative tutorials, and excellent networking and product demonstrations. Participate in 4 days of Focused Tutorials, Real Life Case Studies, Paper Sessions, Automated Tools/Techniques (Computer) Workshop, & Exhibits and go home with the vision and tools to add value to your job performance and your company’s product line.

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- Risk Management Principles and Techniques
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- Introduction to Fault Tree Analysis
- Intro to RAM Management
- Accelerated Reliability Demonstration and Assurance Tests
- Advances in Field Reliability Estimation
- Fundamentals of Failure Modes and Effects Analysis
- Empirical Methods for Process and Equipment Prognostics
- Reliability Demonstration: Theory and Applications
- Software Reliability Applications
- System Safety in a Variety of Industries
- Statistical Warranty Forecasting

. . .and more

Topical Areas: (23 technical sessions)

- Software for R&M
- Math Techniques
- Management and R&M
- R&M Tutorials
- Maintainability/Testability
- Simulation Modeling
- CAE/Concurrent Engineering
- Screening & Failure Analysis
- Int’l R&M Standards
- FMECA/Fault Analysis

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ASIA-PACIFIC EMC WEEK

2010 Asia-Pacific Symposium on Electromagnetic Compatibility & Technical Exhibition on EMC RF/Microwave Measurement & Instrumentation

April 12-16, 2010 Beijing, China

Beijing International Convention Center

- 18 Invited Sessions
- 3 Topical Meetings
- 60 Sessions
- 14 Workshops & Tutorials

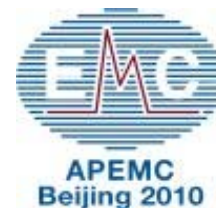
This international symposium covers the entire scope of electromagnetic compatibility. Sessions on: - EMC Management - EM Environment - EMC Measurement Techniques - EMC Standards & Regulations - Lightning Protection - System-Level EMC and Protection - Power System EMC and High Power EMC - Antenna and Wave Propagation - Transportation EMC - PCB & Electronic Packaging EMC and SI - Semiconductor Device and IC EMC - Signal Integrity and Power Integrity - Computational Electromagnetics - Wireless Communication EMC - Bio-Medical Electromagnetics - Nanotechnology for EMC

Exhibition & Sponsorships

The **Technical Exhibition on EMC and RF/Microwave Measurements and Instrumentation** will be the major accompanying event of Asia-Pacific EMC Week. The Technical Exhibition is a must-attend for all major manufacturers and distributors of EMC-related equipment and tools, such as: measurement and EMC test systems, protective devices and components, RF/microwave instrumentation, electromagnetic analysis/synthesis software, etc.

For further information about exhibiting, please contact:

hjun@tsinghua.edu.cn

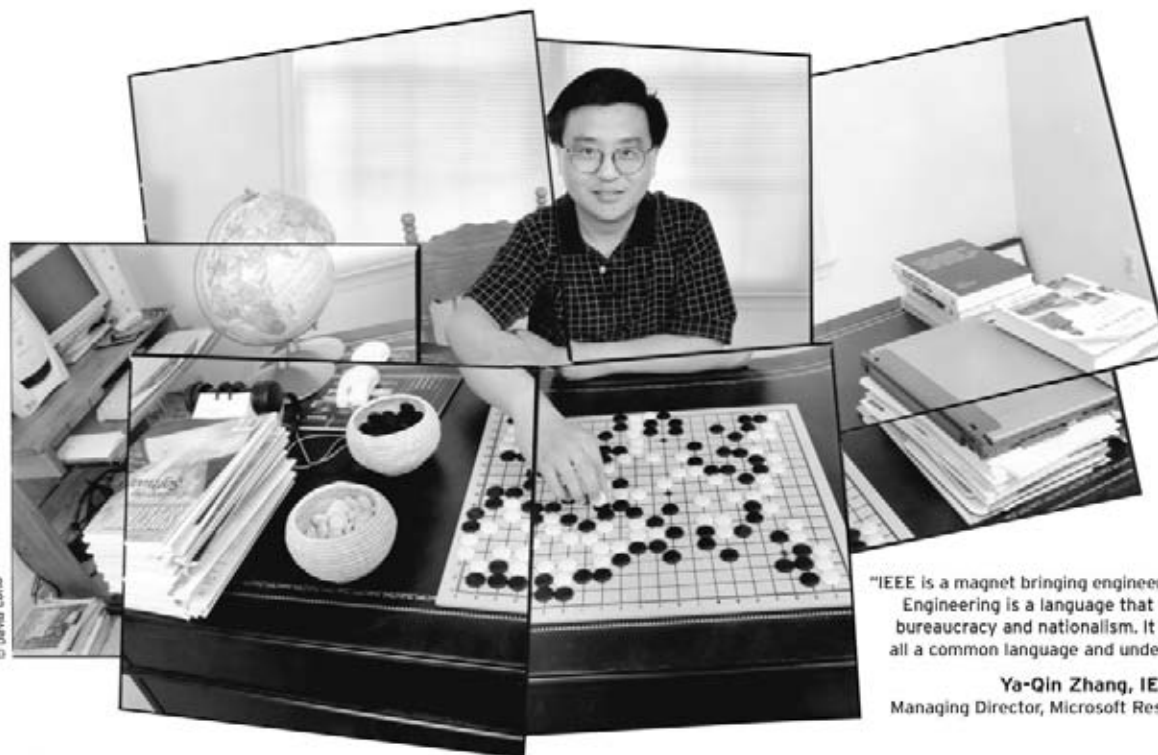


14 Workshops and Tutorials

Electromagnetic Bandgap Structures for Power/Signal Integrity in High-Speed Digital - Power Distribution Network Design for High-Speed - Electronic Package Signal Integrity and EMI Modeling - Electromagnetic Fundamentals for the EMC Engineer - Global EMC Compliance Fundamentals - Grounding Fundamentals and Application from Circuit to System - Radio Frequency Exposure Safety Concerns: Research, Standards, Regulatory Status and Risk Communication - Lightning, Earthing and EMC - Initiation to Modeling and Simulation of EMC of Integrated Circuits - Professional Excellence of EMC Practitioners through Certification - Achieving EMC to Help Control Functional Safety Risks - Global Testing Requirements for Telecommunication Equipment - Microwave Integrated Circuits Design Essentials - Numerical Inversion of Laplace Transform: Its Theory and Application in Transient Analysis of Electromagnetic Pulses

Please see details on the symposium website

www.apemc2010.org



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Ya-Qin Zhang, IEEE Fellow
Managing Director, Microsoft Research Asia



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THURSDAY January 7, 2010

Value-based Scheduling: Get your Organization's Priorities Straight

Speaker: Rino Jose, PhD, Lakeway Technologies
Time: Networking at 6:00 PM; Management Forum at # 6:30 PM; Dinner at 7:15 PM; Presentation at 7:45 PM
Cost: \$10 member/\$13 non-member through 1/5; \$3 more at door
Place: RAMADA Silicon Valley, 1217 Wildwood Ave, Sunnyvale
RSVP: via website
Web: www.ieee-scv-tmc.org

Rino Jose is the principal co-founder of Lakeway Technologies, a company that develops web-based enterprise software for Engineering groups. He has developed software and managed software teams professionally for over 15 years. As a management consultant, he has led turnarounds for multiple engineering teams and is skilled at defining and establishing processes to yield consistent and predictable execution. Rino holds a B.S. from U.C. Berkeley and a Ph.D. from the University of Pennsylvania with cross-disciplinary focus between Engineering, Computer Science, and the Wharton Business School.

A key management challenge today is juggling multiple projects in the face of shifting priorities and overcommitted teams. Studies show that multi-tasking and context switching lead to suboptimal performance and execution, but is single tasking enough? In order for single tasking to be effective, people must know which tasks bring the most value to the organization, a deceptively simple problem. Common strategies, such as assigning revenue to tasks or prioritizing by ROI, are difficult to use in practice and ignore a crucial factor: the value of time.

"Value-based scheduling" is a new approach that integrates product value information with engineering and project information to assign a "cost of delay" to every task in an organization. Using this technique, individuals' tasks can be automatically prioritized by value so that everyone knows which tasks have the biggest impact on the organization. This technique can also be extended to scheduling an entire project portfolio by value, integrating marketing and engineering updates automatically. The resulting schedules are load-leveled and have realistic completion dates that maximize the value of the project portfolio.

This presentation introduces the concept of value-based scheduling and demonstrates its use in engineering development projects.



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TUESDAY January 12, 2010

A New Paradigm for Exchange Bias in Polycrystalline Films

Speaker: Kevin O'Grady, The University of York
(2010 IEEE Magnetics Society Distinguished Lecturer)

Time: Networking and pizza at 7:00 PM;
Presentation at 7:30 PM

Cost: none

Place: Western Digital, 1710 Automation Parkway,
San Jose

RSVP: not required

Web: ewh.ieee.org/r6/scv/mag

Prof. Kevin O'Grady was educated at The University of Wales in Bangor studying for a degree and a PhD in Physics. Subsequently he was employed as a junior professor in Bangor, Loughborough University of Technology and subsequently in the School of Electronic Engineering at Bangor where he achieved a full professorship. In the year 2000 Prof. O'Grady relocated to the Physics Department at The University of York. Prof. O'Grady's work concentrates on magnetisation reversal in a wide range of materials but particularly those finding application in the information storage industry i.e. magnetic hard disk drives.



In his early career Prof. O'Grady studied fundamental fine particle magnetism utilizing colloidal dispersions or ferrofluids as the medium for study. His current research interests are in the field of materials for hard disks but also in exchange bias materials where an antiferromagnet is grown in contact with a ferromagnet and is used to pin one layer in a GMR stack in disk drive read sensors. It is this subject that will be the basis of the Distinguished Lecture. Prof. O'Grady has published over 250 refereed works on the subject of magnetisation reversal. He is a former President of the IEEE Magnetics Society and an Editor of The Journal of Physics D: Applied Physics. He has been associated with the Intermag Conference organization, being ProCom Co-chair in 1996, 2002 and 2008. He is the General Chair for the 2010 Joint Conference. He is also the founding Director of the recently formed York Materials Research Institute.

The phenomenon of exchange bias has remained something of a mystery since it was first discovered in core shell particles in 1956. Over the subsequent years many different models have been attempted to try and explain this effect, most of which agree with some experimental data that can be found in the literature. However, no single theory has ever been able to put a theoretical line consistently through data for different systems.

In this lecture the reason for our inability to explain exchange bias will be reviewed. Subsequently a new paradigm to explain exchange bias in sputtered polycrystalline films will be presented. This new paradigm is based on an original granular model due to Falcomer and Charap. The basis of the new paradigm is that very careful thermal and magnetic cycling is required to ensure that the order in the antiferromagnetic grains is controlled carefully. Without such careful control, reproducible data cannot be obtained.

These measurement procedures, which are time consuming and complex, we refer to as the York Protocol and have been developed over the last 9 years. It will be shown that using the York Protocol and an extension of the former granular model, effects such as the film thickness dependence and grain size dependence of exchange bias can be fully explained with an excellent fit between theory and experiment. The York Protocol also allows for the measurement of the anisotropy constant of antiferromagnetic grains.

The above model allows for an understanding of the behaviour of the individual AF grains in detail. Since the behaviour of the "bulk" of the antiferromagnetic grains is now known, preliminary data describing the behaviour of the interface spins can now be distinguished from the behaviour of the bulk. Possible mechanisms for the behaviour of the interfaces themselves will also be presented.

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The Smart Packet Core for 3G and 4G Mobile Networks

Speakers: Rehan Jalil, Sr VP Mobile Internet, Tellabs; Jay Iyer, Distinguished Engineer, Cisco Systems; Sameer Herlekar, IEEE ComSoc SCV Technical Activities Director

Time: Pizza and Presentations at 6:00 PM

Cost: \$2 donation requested for pizza and soft drinks

Place: National Semiconductor, Building E, Conference Room, 2900 Semiconductor Dr, Santa Clara

RSVP: by Jan. 11 by email to luchang@ieee.org

Web: www.cpmt.org/scv

Rehan Jalil is senior vice president, mobile Internet, at Tellabs. In this role, he is responsible for mobile Internet products and business at Tellabs. Rehan joined Tellabs through the company's acquisition of WiChorus in December 2009, where he was the founder and chief executive officer. He led WiChorus through inception, venture funding, product delivery, partner alliances, brand creation, major customer wins and support. Previously, he was chief architect at Aperto Networks, where he led development of broadband wireless silicon and carrier-grade equipment.

Jay Iyer is a distinguished engineer at Cisco Systems. He is currently responsible for setting Cisco's mobility products technology strategy. He has over 17 years of experience in designing and developing products in routing, switching, wireless and service aggregation. He holds numerous patents in the area of network and wireless convergence. Jay holds a Bachelor of Technology from the Indian Institute of Technology, Madras, and a Masters from Ohio State University.

Sameer Herlekar current research interests are green radio, quantum information processing and optimal hardware/software partitioning of communication receivers. Dr. Herlekar was a Systems Engineer with Mediaphy Corporation, San Jose, where he designed and developed chip sets for multimode mobile DTV receivers. He is an active manuscript reviewer for the IEEE Transactions on Broadcasting, IEEE Transactions on Vehicular Technology, IEEE Communications Letters and for major IEEE ComSoc conferences. Sameer received a Ph.D. from LSU.

The mobile packet core is the functionality that ties together a mobile Radio Access Network (RAN) and the IP routers in the network backbone. Its importance is exemplified by two recent acquisitions in recent months. Cisco Systems bought 3G and LTE gateway specialist Starent Networks, while Tellabs has entered the wireless core market with the acquisition of WiMax access service network (ASN) gateway vendor WiChorus.

In the last year or so, there has been a major transformation in how mobility is perceived by consumers and delivered by wireless networks. As mobile applications and consumer expectations grow, this puts a rather taxing requirement on the network – scaling, throughput, and keeping costs lower. Jay Iyer, Distinguished Engineer, Cisco Systems will talk about how all IP network intelligence plays a key role in the mobile Internet transformation.

Rehan Jalil, Senior Vice President, Mobile Internet Division, Tellabs, will discuss the need for a smart packet core architecture in today's emerging mobile networks so operators can reduce operation expenditures, maximize use of existing network assets and create new ways to monetize the content flowing through the mobile network. A smart 4G core makes all of these goals realities by being able to accommodate the dramatic increase in mobile Internet traffic, analyze the traffic loads and dynamically adapt traffic management policies, and differentiate QoS and enable accounting based on content. As a result of this approach, mobile operators can create an avenue for additional end-user Internet usage capacity, and ultimately the opportunity to increase ARPU. Jalil will elaborate about how this intelligent core services engine approach is alleviating the additional network demands of network operators today, and share an innovative new solution that can reduce costs and increase revenues such that operators can profit from the mobile data explosion rather than be overwhelmed by it.

A lively panel session will follow these presentations. The speakers and moderator will address the role of the mobile packet core as wireless networks evolve from 3G to 4G. They will also provide their prospective on the outlook for mobile broadband and fixed BWA in India.



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WEDNESDAY January 13, 2010

High-Reliability Through-Silicon Via (TSV) Solutions for Image Sensor Packaging

Speaker: Belgacem Haba, Fellow and Chief Technology Officer, Interconnect, Components & Materials (ICM), Tesser
Time: Optional dinner at 6:30 PM; Presentation (no cost) at 7:30 PM
Cost: \$25 if reserved by Jan. 11; \$30 at door
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: via our DoubleKnot reservation site
Web: www.cpmt.org/scv

There is no doubt that the potential of imaging is astronomical. Current and potential markets include digital still cameras, business applications, Webcams, cell phone cameras, security cameras, gaming, video, automotive and toys. In 2009, the industry shipped 2.5 billion image sensor units with an average selling price of \$5 – providing a total addressable market of \$12B. This presentation will discuss image sensor and camera module trends and growth. It will trace the growing movement in the image sensor market from chip-on-board to wafer-level packaging for cost savings and other advantages. It also will trace the image sensor evolution toward wafer-level packaging and introduce through-silicon via (TSV) wafer-level chip-scale packaging, and how to address the barriers to adoption with a new approach.

Belgacem Haba is a Tesser
Fellow and chief technology officer for the Interconnect, Components & Materials (ICM) division. He is responsible for directing research and strategic development in leading-edge packaging technology. Haba came to Tesser from SiliconPipe Inc., a high-speed Internet start-up company which he co-founded. During his 20 year career, he has held management positions in research and development at Rambus, NEC Central Research Laboratories, and the IBM T.J. Watson Research Center. He has published over 100 articles, holds 100 U.S. patents and more than 140 international patents and patent applications. He is a member of the IEEE Components, Packaging, and Manufacturing Technology Society. Haba holds a bachelor's degree with honors in physics from the University of Bab-Ezouar, Algeria, master's degrees in applied physics and materials science and a doctorate in materials science and engineering from Stanford University.



TUESDAY January 19, 2010

Nanotechnology in 2010 and Beyond: Beating the Recession, Launching Big Ideas

Speaker: Mark Bünger, Director of Research, Lux Research
Time: Light lunch at 11:30AM; Presentation 12:00 noon
Cost: IEEE Members and Students \$5; Non-Members \$10
Place: National Semiconductor Bldg E-1 CMA Room. 2900 Semiconductor Drive, Santa Clara
RSVP: from the website
Web: www.ieee.org/nano

Mark Bünger is a Director of Research at Lux Research, which he joined 4 years ago. Prior to Lux, he had 14 years of business strategy experience as a management consultant and technology analyst as a Principal Analyst at Forrester Research, Managing Director at Icon Medialab, and Senior Consultant at Accenture. Mark's education includes International Marketing at Mälardalen Polytechnic in Sweden, and Market Research at the University of Texas in the U.S. He also studied biochemistry through the University of California at Berkeley's extension program and assists in a bioengineering lab at UCSF.

The economic downturn has hit key nano-enabled product segments hard – in particular, auto, construction, and electronics. Lower output and slower technology adoption in these industries will ripple up the value chain to nanointermediates and nanomaterials, leading to total revenue from products incorporating nanotechnology of \$2.5 trillion in 2015 - down 21% from our previous projections. The changes will put large corporations in the driver's seat, force start-ups to break even or bust, and demand creative action from governments. At the same time, big ideas are on the horizon: Academic research in nanotech is growing at ten times the rate of scientific study overall, and companies are aligning themselves with research labs to stake claims on early-stage technologies. Our review of academic nanotech research finds Asian countries leading, carbon nanotubes and coatings/composites applications on the downswing, and graphene and life sciences applications rising. From the body of research, we identify five promising technologies - nanomotors, metamaterials, silicon nanowire thermoelectrics, graphene transistors, and plasmon-enhanced solar cells - that stand poised to have the highest commercial impact. In this presentation, Lux Research's Mark Bünger will present market data, technology trends, and the latest in applications relevant to the IEEE community, including sensors and diagnostics, nanoelectronics, coatings, and other areas.



TUESDAY January 19, 2010

What Everyone Should Know About China

Speaker: Rosemary Coates, President, Blue Silk Consulting
Time: Presentation 7:00 PM
Cost: none
Place: KeyPoint Credit Union, 2805 Bowers Ave., Santa Clara
RSVP: not required
Web: www.CaliforniaConsultants.org

Rosemary Coates is President of Blue Silk Consulting. She has become an expert in sourcing and manufacturing in China by way of her 25 years of supply chain experience, much of it spent living and working across Asia.



Prior to Blue Silk Consulting, Rosemary was a Senior Director at SAP, the Supply Chain Practice Leader at KPMG Peat Marwick and at Answerthink, and a Regional Manager at Hewlett-Packard. She has nearly 20 years of consulting experience, with over 80 clients worldwide.

Ms. Coates is a Licensed United States Customs Broker and a Lifetime Credentialed Instructor, California Colleges and Universities. She taught Management, International Business and Importing and Exporting for ten years.

Rosemary earned an MBA in Finance and Operations Management from the University of San Diego, and a BS in Logistics from Arizona State University. Her new book is **42 Rules for Sourcing and Manufacturing in China**.

Nearly 40% of the world's production is now in China, and it is the world's fastest-growing middle-class market. Because our everyday lives are affected by what goes on a hemisphere away, a fundamental understanding of this market is important to anyone wishing to be better informed about what their future holds.

Doing business in China is tougher than you think. Not only is the culture vastly different, but China's experience in manufacturing is still developing. The best way to quickly come up to speed on these differences is to learn from the experience of others.

By way of over 20 extraordinary executive interviews, Rosemary Coates captured the essence of sourcing and manufacturing in China in her new book. This talk will provide attendees with an important cultural perspective by covering the most important aspects of this book.

WEDNESDAY January 20, 2010

SMRT (Single-Molecule, Real-Time) Biology

Speaker: Jonas Korlach, PhD, Pacific Biosciences

Time: Optional no-host dinner at 6:15 PM;
Presentation at 7:30 PM

Cost: none

Place: Optional dinner at Nexus Cafeteria;
meeting at Room M-114, Stanford
University Medical School

RSVP: not required

Web: www.ewh.ieee.org/r6/scv/embs

Jonas Korlach received a Diplom (Masters) degree in biology from Humboldt University (Germany) in 1996, and a PhD in biochemistry, molecular and cell biology from Cornell University in 2003 where he initiated the technology development on SMRT DNA sequencing as a collaboration between the labs of Watt Webb and Harold Craighead. After a short postdoc at the same institution and as a technical consultant to Pacific Biosciences, continuing with this research, he joined Pacific Biosciences as employee #3 after it received the first round of venture capital funding to commercialize the method. He currently holds the title of Principal Scientist at the company, supporting commercial development of the SMRT DNA sequencing system, and performing research aimed at enabling new applications within the 'SMRT Biology' realm.

Organisms can be viewed as dynamic, highly modular, and adaptive systems able to reconfigure themselves as conditions demand. The scientific community is increasingly recognizing that multiple data sources (e.g., DNA, RNA, protein and metabolite levels, etc.) and sophisticated computational approaches that integrate diverse data are required to uncover the hierarchy of molecular, cellular, and tissue-based networks defining these complex physiological transitions, sometimes leading to disease. While a significant technological revolution in biology has led to this realization, limitations in the available technologies have hampered the ability to embrace this scale of complexity. In order to fully realize the promise of personalized medicine, scientists require a means to obtain a comprehensive understanding of the fundamental building blocks of biological systems.

SMRT™ (Single Molecule Real Time) Biology is the application of Pacific Biosciences' transformative detection platform enabling the real-time monitoring of biological processes at single-molecule resolution. The first commercial application for this transformative platform is SMRT DNA sequencing (available in 2010). Pacific Biosciences has begun expanding internal research programs and developing collaborations for additional 'SMRT Biology' applications and bioinformatics tools that will allow scientists to acquire new, fundamental knowledge about the molecular dynamics of life. These include simpler and more direct solutions for RNA sequencing, methylation sequencing, and even the largely uncharted real-time observation of protein translation.

Jonas will first highlight the importance of a comprehensive determination of DNA, RNA and protein sequences and abundances for the understanding of life processes. He will then describe the principles of the underlying SMRT technology in the context of an historical account of its development which is an example of both the power of multidisciplinary scientific endeavors, and the potential of transferring an academic research project into an industrial organization environment.

The current performance of the SMRT DNA sequencing system will be presented with an emphasis on the enablement of entirely new possibilities of inquiries into biological systems, followed by an outlook of projected performance potentials and implications for the changes it will bring with regard to our perception on medicine.

THURSDAY January 21, 2010

Integrated Circuit Design with Nano-Electro-Mechanical Switches

Speaker: Prof. Elad Alon, UC-Berkeley
Time: Refreshments at 6:0 PM; Presentation at 6:30 PM
Cost: none
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Dr., Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/ssc

No matter how slowly they are allowed to run, digital logic gates implemented with CMOS transistors have a well-defined minimum energy that they must dissipate for each operation they perform. This minimum energy dissipation in CMOS can be traced back to the imperfection of transistors as switches - i.e., that their subthreshold slope is limited by kT/q . In contrast, switches based on mechanically making or breaking electrical contact can achieve zero leakage and infinite subthreshold slope, and hence may some day enable substantial improvements in energy efficiency. However, realizing this goal requires that the underlying circuits are tailored to the characteristics of these switches. Hence, in this talk I will describe such mechanical switch-optimized circuit architectures and then quantify the energy, performance, and area tradeoffs of these designs in comparison to CMOS.

Prof. Elad Alon received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University in 2001, 2002, and 2006, respectively. In Jan. 2007, he joined the University of California at Berkeley as an Assistant Professor of Electrical Engineering and Computer Sciences, where he is now a co-director of the Berkeley Wireless Research Center (BWRC). He has also held visiting positions at Intel, AMD, Rambus, Hewlett Packard, and IBM Research, where he worked on integrated circuits for a variety of applications using bulk and SOI processes from 130nm down to 32nm. His research focuses on the design and implementation of energy-efficient integrated systems and the circuits/technologies that comprise them.

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THURSDAY January 21, 2010


Robot Team Coordination and Simultaneous Localization and Mapping (SLAM)

Speaker: Dr. Regis Vincent, Software
Commercialization team, SRI International
Time: Presentation at 7:00 PM
Cost: none
Place: CMU-SV, Building 23, Moffett Field,
Mountain View
RSVP: not required
Web: ewh.ieee.org/r6/scv/css

Dr. Regis Vincent is currently leading the Software Commercialization team at SRI International. He is an experienced researcher and engineer and has produced commercial-grade software systems. His recent project includes building the first commercial robotic solution for mapping and localization. The Karto mapping system works on over 20 different robots and is compatible with all laser range finders. The Karto system grew out of the Centibots that Dr. Vincent was co-leading. At the time, the Centibots project was the largest deployment of robot in the world. Since joining SRI, Dr. Vincent has been working on monitoring and adaptation for physical systems, and on the Unmanned Combat Air Vehicle project. The goal of the project is to demonstrate the collaboration and adaptation of a team of UCAVs and UGVs (Unmanned Ground Vehicle) to achieve tactical missions. Dr. Vincent received his Ph.D. from the University of Nice, France in 1997. His research interests are real-time artificial intelligence, from scheduling, planning to negotiation. He has published over 30 papers in peer-reviewed conferences and journals. He has also co-edited a book on multi-agent coordination "Coordination of Large-Scale Multiagent Systems" published by Springer.

2D laser SLAM (Simultaneous Localization and Mapping) has reached a maturity that has allowed the development of commercial applications. The testing of SRI International's SLAM algorithm for commercial projects will be described and how the industry's requirements help to advance the SLAM algorithms. For example, buildings over 1 million square feet have not be scanned before, or all seven floors of the same buildings.

The speaker will describe a control method for the coordination of robot teams, or multi-agent coordination, and outline current research in utilizing such teams for SLAM.



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THURSDAY January 21, 2010

Channel Surfing: Managing Propagation in Broadband Wireless Systems

Speaker: Dr. Derek Shaeffer, InvenSense
Time: Pizza & Networking at 6:00 PM;
Presentation at 7:00 PM
Cost: none
Place: Cogswell Polytechnical College, 1175
Bordeaux Drive, Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/aps

Broadband wireless systems such as WiMAX and LTE are poised to revolutionize mobile internet access. However, with downlink data rates in the 10-100Mb/s range and cell radii on the order of 1-5km, these emerging, carrier-class broadband wireless systems face significant challenges when it comes to managing the deleterious effects of wireless propagation. These challenges are met in both systems with OFDMA modulation which is uniquely suited to the vagaries of the wireless channel. In this talk, we will explore the propagation factors that make broadband wireless communication such a challenge and how OFDMA-based systems manage and mitigate these factors.

Derek K. Shaeffer received the BSEE degree from the University of Southern California in 1993, the MSEE degree from Stanford University in 1995 and the Ph.D. degree from Stanford University in 1999, for which he did early work in the field of RF CMOS, demonstrating the world's first CMOS GPS receiver. His 1997 paper on CMOS low-noise amplifiers is among the most frequently cited papers in the Journal of Solid-State Circuits with over 150 citations to-date. He is the author or co-author of eleven issued patents and several pending patents, twenty papers and a book on CMOS RF design. He has worked professionally in the fields of test instrumentation, semiconductor memory, optical and wireless communications. Dr. Shaeffer has also served as Associate Editor of the Journal of Solid-State Circuits. He is currently a Director of IC Design with InvenSense, Inc., where his work is focused on MEMS gyroscopes.

FRIDAY January 22, 2010

Half-Day Seminar: Patents for Engineering Consultants: The Basics, Your Opportunities, and Your Risks

Speakers: Joel Williams, emLinux (Embedded Linux Design Services); and Tal Lavian, Ph.D., Innovations-IP (Patent Innovations Consulting)

Time: 8:30 AM - 11:30 AM

Cost: \$49 for members of IEEE and other National Engineering Societies (\$29 for Webinar); \$69 for non-members (\$39 for Webinar)

Place: KeyPoint Credit Union, 2805 Bowers Ave., Santa Clara (limited to first 50); Webinar is on Internet

RSVP: Visit the EventBrite website

Web: patent1.eventbrite.com

Joel Williams has been a consultant for over 20 years, specializing in communications and embedded systems. He has developed communications systems for clients using a wide range of technologies including Wi-Fi wireless protocols and network switches. Embedded systems development has focused primarily on embedded Linux systems, and has leveraged Joel's broad experience with other embedded technologies and Unix.

Joel has worked with standards organizations, and has established product certification testing programs. He also provides patent review, litigation support, forensic analysis and expert witness services in legal matters. Joel holds several patents.

Joel is currently Vice-Chair of CNSV. He was CNSV Secretary in 2007-2008, and was CNSV Treasurer in 2005-2006. He is a senior member of IEEE.

Dr. Tal Lavian was a principal scientist at Nortel Networks Research Lab and a visiting scientist at UC Berkeley Engineering. He identified prospective business and technology ideas, turning them to new networking products. He was the Principal Investigator for three US Department of Defense (DARPA) projects.

Areas of Consulting include Data Networking, Telecommunications, Network Architecture, Intellectual Property, IP, IPR, Inventions, Patents, Innovations, Litigation Consultant, and Trade secrets.

He is a prolific innovator, co-inventing over 40 patents issued and pending. He is also the co-author of over 25 scientific publications, journal articles, and peer-reviewed papers. Dr. Lavian received Top Talent award and Top Inventors award from Nortel.

How well do you understand patents, the opportunities they create, and the risks that patents can create for your consulting practice?

Consultants are at the top of their field. As such they need to know about intellectual property: patents and trade secrets. Patents provide opportunities for income and career advancement as well as responsibilities to help and protect your clients and yourself.

In this interactive seminar and panel discussion, you will learn:

- Basics you need to know
- Risks that patent issues create for engineering consultants (you as a defendant, you as a witness for a client)
- Intellectual property ownership and expert witness business opportunities that patents can create for engineering consultants
- How hardware and software companies, startup companies, and individuals can use patents to their advantage to protect their intellectual property
- Your clients' objectives in establishing/negotiating patent rights with consultants who are technical experts
- The various parts of a patent and key issues to understand about each part
- How co-authoring patents enhances your resume
- Brief description of the patent process that can last for several years
- Brief descriptions of actual legal cases where patents have been asserted or defended in ways that impacted engineering consultants

You will understand:

- How to recognize intellectual property
- How patents are used and the patent process
- How to "read" patents
- Consultants and trade secrets
- Ownership of IP
- When you might own intellectual property to license to clients (not as often as you wish). Or, when you might share in a client's/partners' patent (not as often as you wish)
- When it makes sense to write a new patent in your name
- Risks that your clients have associated with patents
- Risks that you have associated with patents
- Other opportunities that patents can create for you
- What questions to ask your patent attorney

TUESDAY January 26, 2010

Cogeneration: An Electrical Perspective

Speaker: Diep Nguyen DTN Engineering Inc.
Time: Social at 5:30 PM, Presentation at 6:00 PM, Dinner at 7:00 PM
Cost: \$25 (at the door); \$10 for student members (first 5)
Place: Sinbad's Restaurant, Pier 2 The Embarcadero, San Francisco
RSVP: Please email Frank Sylvester, frank.sylvester@sfdpw.org for reservations and to qualify for the drawing.
Web: www.e-grid.net/docs/1001-sf-ias.pdf

Diep Nguyen has been a practicing electrical engineer for more than three decades. He is currently working for DTN Engineers Inc. as a consulting electrical engineer. He is a senior member of IEEE, past Chair of OEB PES, and currently R4 and R6 PES Regional Representative.

Cogeneration is still alive and well in the minds of many practicing electrical engineers. By conventional definition, a cogeneration plant produces both steam and electricity from a same fuel source. As long as a cogeneration plant or a power generation plant that has electrical-mechanical machineries such as gas turbines, reciprocal engines, steam turbines, combustion turbines, micro-turbines etc., the electrical power system design approach for these systems in general will be identical in many ways.

This presentation discusses electrical design aspect of cogeneration plant or similar power generation plant with specific consideration for interconnection with utility grid as an application of distributed generation. It will focus on practical design of available modern, low and medium voltage electrical switchgear with multi-function protective relaying, short circuit rating, arc-resistant medium voltage metal-clad switchgear, and essential plant's auxiliary systems.

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TUESDAY January 26, 2010

Non-adiabatic Spin-torques in Narrow Magnetic Domain Walls

Speaker: Dafiné Ravelosona, CNRS, Orsay, France

Time: 3:00 PM

Cost: none

Place: Lawrence Berkeley National Labs, Berkeley

RSVP: Please respond by email with name, company to Peter Fischer,

PJFischer@lbl.gov by January 22

Web: ewh.ieee.org/r6/oeb/mag

Dafiné RAVELOSONA is an experimentalist physicist and he is currently working within the "Nanospintronics" group at Institut d'Electronique Fondamentale (IEF), in Orsay (France). After a Ph. D. in Solid States Physics (1995) and a post doc fellowship at CNM in Madrid (Spain), he became a permanent research member of CNRS in 1998 at the University of Orsay. From 2004 to 2005, he joined as an invited scientist the research center of Hitachi Global Storage Technology in San José. He is presently coordinator of a collaborative national funded project in charge of developing highly integrated spintronics devices based on magnetic domain walls driven by a spin polarized current. He has over 12 years of experience of magnetic thin-films growth, nanodevices development, magnetotransport phenomena and nanomagnetism. His work has mainly focused on transport phenomena in nanostructures with perpendicular anisotropy for applications to logic and solid state memories.

Torques appear between charge carrier spins and local moments in regions of ferromagnetic media where spatial magnetisation gradients exist. Understanding the magnitude and orientation of such spin-torques is an important problem for spin-dependent transport and current-driven magnetisation dynamics, particularly so for domain-wall motion which underlies a number of emerging spintronic technologies. Here, we report an experimental measurement of the non-adiabatic spin-torque component β in perpendicularly magnetised films with narrow domain walls (1-10 nm)^[1]. By studying thermally-activated domain wall depinning, we deduce from the variation of the Arrhenius transition rate with applied currents. Surprisingly, we find β to be small and relatively insensitive to the wall width, which stands in contrast to predictions from transport theories. In addition, we find β to be close to the Gilbert damping constant α , which, in light of similar results on planar anisotropy systems, suggests a universal origin for the non-adiabatic torque.

[1] Nature Physics, doi:10.1038/nphys1436 (2009)

TUESDAY January 26, 2010


Codes, Standards and Listings: Who Requires What, and Why

Speaker: John Taecker, P.E., Underwriters Laboratories Inc.
Time: Optional Dinner: 5:30 – 6:45 p.m. at El Torito Mexican Restaurant; Mtg at Applied Materials, Bowers Café at 7:00 PM
Cost: none, for meeting
Place: El Torito Mexican Restaurant, 2950 Lakeside Drive, Santa Clara; mtg at Applied Materials, Bowers Café, 3090 Bowers Ave, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/pses

There are many installation codes and product testing standards that apply to products. How can you determine what codes and standards effect your product? What reliable resources are available? Does the installation code influence the testing standard, or does the standard influence the code? How are codes and standards developed, and are there any opportunities to provide input? What products are required to be Listed? Why are the products required to be Listed? Learn who requires products to be certified by a third-party agency, what requirements are used, how a product is certified, and where information about certifications can be found.

Discussion will include both the safety requirements, but also the new requirements under development for sustainable ("green") buildings and energy efficiency.

John Taecker, P.E. has worked for Underwriters Laboratories Inc. for 25 years. He has a BS in Mechanical Engineering from Cal Poly, San Luis Obispo, and is a California Registered Professional Engineer in Safety Engineering. He has served on various building, mechanical, and plumbing code development committees, and actively participates in all levels of the code development process for ICC and IAPMO. He is a nationally recognized speaker on electrical, building, mechanical, and plumbing products and installations.



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THURSDAY January 28, 2010

Thin is In: Thinning of IC Chips

Speaker: Annette Teng, Ph.D., Corwil Technology Corp.

Time: Registration at 11:30 AM; Buffet lunch at 11:45 AM; presentation (no cost) at 12:15 PM

Cost: \$15 if reserved by Jan 26; \$20 at door; vegetarian available

Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara

RSVP: Through the website link

Web: www.cpmt.org/scv

Silicon chips as thin as 0.050um are becoming common. Many manufacturers have achieved success in their development of thin die. This talk will focus on singulation and thinning techniques to create silicon crystal slices which can withstand the assembly, packaging and field service. The talk will discuss using die attach films (DAF) to support the ultra-thin dies and to stack dies vertically. The speaker will also address the shifting landscape of the component manufacturing industry, such as the increased use of laser cutting and the outlook for DAF films replacing traditional die attach epoxy.

Annette Teng graduated with M.Sci. and Ph.D. in Materials Engineering from University of Virginia in Charlottesville. Her first job was at Signetics Corp. where she was responsible for failure analysis, development, manufacturing and reliability engineering of both plastic and hermetic packages. She worked at Linear Technology Corp. from 1990 to 1996 in the package assembly for military and commercial products. In 1997 she moved to Hong Kong and launched the Electronic Packaging Lab at The Hong Kong University of Science and Technology with Government funding for flip chip and materials R & D. In 2000, she joined CORWIL Technology Corp, a prototyping assembly contractor located in Silicon Valley. She has overall responsibility in the areas of backgrind, dicing, die attach and flip chip production. She is program manager and staff scientist in charge of developing new manufacturing processes for advanced packaging and wafer level packaging. Annette is very active in IEEE-CPMT and has published papers at ECTC, IEMT and EMAP conferences.

FRIDAY January 29, 2010

**One-Day Seminar:
3D Interconnect -
Shaping Future Technology**

Speakers: experts from academia and the
semiconductor industry; to be announced
Time: 9:00 AM to 5:00 PM
Cost: Free. Refreshments and lunch provided
Place: Hyatt Regency Hotel, Santa Clara
RSVP: Through the website link
Web: www.ewh.ieee.org/r6/scv/eds

The demand for higher densities, smaller form factors, and greater functionality, and the quest for developing post-CMOS technologies is spurring ongoing research in a wide variety of wafer-scale integration techniques. This program brings together experts from academia and the semiconductor industry to examine the state of research into 3D interconnect, development of unit-process and integration, and production qualification.

WEDNESDAY February 10, 2010

Large-Scale Print Manufacturing of Complex, Miniature 3D Structures

Speaker: Arthur Chait, President and CEO, EoPlex Technologies, Inc.
Time: Dinner at 6:00 PM (new time!);
Presentation at 6:45 PM
Cost: \$20 if reserved by Feb. 8; \$25 after & at door; vegetarian available; no cost for presentation only
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: Through the website link
Web: www.cpmt.org/scv

Arthur L. Chait, President and CEO, was previously a senior executive of Solectron Corporation, a leading contract manufacturing firm, with revenues in excess of \$12 Billion/year. Chait had responsibility for Solectron's Global Account Organization, representing over 70% of the company's revenue with customers including: Cisco, IBM, Nortel, Dell, Sun, HP, Compaq, Agilent, Ericsson, Lucent, Motorola, Apple, Intel and others. He also had worldwide responsibility for marketing and helped lead Solectron into new markets including automotive, consumer electronics, and industrial. Chait was part of the senior team at Solectron that grew the company from \$6.1 Billion in FY98 to \$18.6 Billion in FY01. Mr. Chait's career also includes SRI International where he was SVP of the worldwide consulting group with a staff of over 600; Zitel Corporation where he was GM and SVP of the software division; Booz Allen & Hamilton where he was Senior Engagement Manager; The PA Consulting Group (UK) where he was GM for North America; and Dresser/Halliburton where he was Director, Product Development.

Mr. Chait is a past recipient of the Steinmetz Medal from GE. He holds two degrees: a BS degree in Ceramic and Materials Engineering from Rutgers University and an MBA in Strategy from the University of Pittsburgh.

Mr. Chait serves on the Boards of Blue Iguana Networks and TechVenture Networks, and was past Board Chair of the Challenge Learning Center, a non-profit organization that assists "at risk" young people in the San Francisco Bay Area.

In this presentation, materials scientist and entrepreneur Arthur L. Chait will share a game-changing print deposition technique for the large-scale manufacture of electronic components and packages. He will discuss the innovative EoPlex process, based on custom printing equipment and proprietary "inks" that carry ceramic, metallic or polymer materials to millions of locations. This technique allows the manufacture of components with integrated chambers, channels, dielectrics, sensors, circuits, reactors, energy scavengers and other features.

Chait will further show how the process allows new design freedoms and advancements that were not available before. Many parts are created simultaneously in large panels at high-speed and low-cost. This new clean-tech process produces complete components that include miniature antennas like those used in cell phones, GPS and other portable devices. A new semiconductor packaging micro-lead frame that offers better performance and lower cost in many portable devices will be launched in the months ahead.

Chait will describe how this print layering additive technique replaces many older processes, such as etching, plating or machining, which either require toxic chemicals or which generate fine particle wastes. He will explain how this platform technology is unique in the clean tech space. In addition to the process being clean, some of the products the company has demonstrated, such as fuel cell parts and energy harvesters, enable small form-factor, alternative energy sources.

TUESDAY February 16, 2010

Technology Trends for Magnetic Storage: What is the Future?

Speaker: Dr. Edward Grochowski, Computer Storage Consultant

Time: Networking and pizza at 7:00 PM;
Presentation at 7:30 PM

Cost: none

Place: Western Digital, 1710 Automation Parkway,
San Jose

RSVP: not required

Web: ewh.ieee.org/r6/scv/mag

Ed Grochowski is a well known speaker on magnetic storage technology. He began his career with IBM's microelectronics silicon activity in New York and later joined the IBM Almaden Research Center where his interests included hard disk drive and component evolutionary trends. Dr. Grochowski holds nine patents and has authored and presented numerous articles on magnetic disk drives and component technology, including a website of storage trend charts. He has a Ph.D. from New York University in Chemical/Materials Engineering. Ed served as Executive Director of IDEMA USA and for over ten years chaired the conferences and technical committees for DISKCON USA and DISKCON Asia Pacific, as well as the prestigious Symposium series. He was a long time coordinator of the 4K byte sector standards committee. Ed is also a member of the IEEE.



As a consultant, Dr. Grochowski has been associated with Hitachi GST, IDC, TrendFocus and Coughlin Associates. With the latter, he co-authored a comprehensive 2008 storage report addressing HDD technology trends and capital equipment requirements for the industry, and plans to publish an update of this work in early 2010.

Today's hard disk drive has evolved through miniaturization into a small storage device with up to 2.5 Terabytes of storage, with the promise of multiterabyte products appearing in the very near future. This storage device, based on reduced form factors and large capacity, is well suited for today's storage applications, from large server units to mobile PC's and consumer based products. The technology which made this storage device possible includes advanced read/write heads which now include PMR, TMR, thin film media, PRML data channels and many other features which have added to the usefulness of HDD's while significantly reducing price per gigabyte. An analysis of this technology will be given as well as projections of where newer advances could extend the applications of magnetic storage products to the future. A comparison of HDD storage to alternative non-volatile technologies including Flash memories and MRAM devices will be discussed. The challenges of advanced processing techniques will be outlined. A major part of the presentation will include trend charts, with technical rationale, to assist in the projecting the future.

WEDNESDAY February 17, 2010

Optical Coherence Tomography – From Bench to Bedside

Speaker: Tony Ko, PhD, Optovue, Inc.
Time: Optional no-host dinner at 6:15 PM;
Presentation at 7:30 PM
Cost: none
Place: Optional dinner at Nexus Cafeteria;
meeting at Room M-114, Stanford
University Medical School
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/embs

Tony Ko received Bachelor of Science degrees in Electrical Engineering & Computer Science (EECS) and Bioengineering from the University of California at Berkeley, a Masters of Science in EECS from MIT, and a PhD in Medical Engineering and Medical Physics from the Harvard-MIT Division of Health Sciences and Technology. Tony performed his PhD research in the MIT laboratory of Prof. James Fujimoto, one of the original inventors of Optical Coherence Tomography. He is currently the Manager of Advanced Development at Optovue, Inc., an ophthalmic medical device company.

Optical Coherence Tomography (OCT) is the optical analogue of ultrasound that was invented about 20 years ago at MIT. OCT provides the ability to acquire cross-sectional images from biological tissue with much better resolution than ultrasound. It was recognized that OCT can have an impact in the field of ophthalmology where high-resolution cross-sectional images of the retina were not available and would be of clinical value. However, it took about 10 years for the market to evolve and the technology to mature before OCT gained acceptance in the field of ophthalmology. Recent scientific advances have dramatically improved the technical performance of OCT and further improved its clinical utility and impact. Today, OCT has become a clinical standard in ophthalmology and an important diagnostic tool for managing retinal diseases. There are now nine companies developing OCT instruments for ophthalmology and many others are exploring applications of OCT technology in clinical fields such as cardiology, dermatology, and gastroenterology.

Tony Ko will discuss the development of OCT from the university research labs to everyday clinical use in ophthalmology at the February 17 meeting of the Santa Clara Valley Engineering in Medicine & Biology Society. The successful transfer of OCT into ophthalmology is an interesting case study in the many factors that contribute to the acceptance of a new technology into medicine.

TUESDAY February 23, 2010

Getting the Most Out of Your Electrical Room

Speaker: Daniel Thompson, Schneider Electric
Time: Social at 5:30 PM, Presentation at 6:00 PM, Dinner at 7:00 PM
Cost: \$25 (at the door); \$10 for student members (first 5)
Place: Sinbad's Restaurant, Pier 2 The Embarcadero, San Francisco
RSVP: Please email Frank Sylvester, frank.sylvester@sfdpw.org for reservations and to qualify for the drawing.
Web: www.e-grid.net/docs/1002-sf-ias.pdf

Is your architect pushing you to size the Electrical Room without room to wiggle? Fear not, because Daniel is here! He will focus on common consultants' FAQs about the 4 main topics of Electrical Room design: (1) Work Clearance, (2) Equipment Sizing, (3) Utility Requirements, and (4) Seismic Concerns. Daniel's presentation will introduce Electrical Room design starting from the basics, but he will provide enough tips & tactics to satisfy the most experienced engineers.

Please join us in welcoming our speaker to San Francisco for what is sure to be an interesting and productive session.

Daniel Thompson graduated from Cal Poly SLO in 2000, and is currently working for Schneider Electric. In addition to assisting consultants, Daniel has worked in Square D's Power Division, configuring switchboards, switchgear, and other electrical distribution equipment. Along with developing resources for consultant use, Daniel regularly fields questions from consultants ranging from code application to proper equipment configuration. Daniel has attended IAS & PES events around the Bay Area, and was on the 2004 IEEE PCIC local committee.