

CHAPTER MEETINGS

SCV-CS - 7/12 | **Future Vehicle Computer System in a Five-Screen World** - information, entertainment, driving assistance ... [\[more\]](#)

SCV-CSS - 7/13 | **Networked Control Systems II: Innovative Topologies for Distributed Motion Control** - ethernet, real-time ... [\[more\]](#)

SCV-ComSoc - 7/13 | **Architectures and Signal Integrity Challenges for 100 Gbps Data Transmission Systems** – bandwidth ... [\[more\]](#)

SF-PES - 7/14 | **Power System Reliability Analysis and Artificial Intelligence** - capital investment, costs, operations ... [\[more\]](#)

SCV-CS - 7/16 | **Emerging Automotive Computing: Engineering in Overdrive** - autonomous vehicles, controls, telematics ... [\[more\]](#)

SCV-Nano - 7/19 | **A Breakthrough in Nanocomposite for High-Capacity Hydrogen Storage** - metal-polymer, cycling ... [\[more\]](#)

IEEE-USA - 7/20 | **Cyber Security in the Electric Utility Sector** - mission critical, reliability, availability, external threats, policy ... [\[more\]](#)

SCV-PELS - 7/20 | **Design and Implementation of Ethernet Magnetics and Power Magnetics using Planar PCB-Based Embedded Ferrite Technology** - inductive components ... [\[more\]](#)

OEB-PES - 7/20 | **Tour of 300kW PV Solar Tracking System** - sun-tracked solar system, operational, short presentation ... [\[more\]](#)

SCV-PV - 7/20 | **From Factory to Field: Developing Utility-Scale PV Projects** - power plants, companies, competition, business ... [\[more\]](#)

SCV-PACE - 7/21 | **Intellectual Property Traps and Opportunities for Employed Future Entrepreneurs** - employee, consultant, ... [\[more\]](#)

SCV-ComSoc+CPMT - 7/26 | **Tour: SMT (Surface Mount Technology) Manufacturing and Engineering** - PCB, design, assy ... [\[more\]](#)

OEB-Mag - 7/27 | **Nanofabrication of Bit-patterned Media by Block Copolymer Directed Assembly** - sub-20nm, self assembly ... [\[more\]](#)

SCV-IT - 9/28 | **The Role of Information Theory in Public Key Cryptography** - research, theory, preparation, training ... [\[more\]](#)

For updated information, visit the
IEEE GRID website: www.e-grid.net

Conference Calendar

July 16: **NFIC: Emerging Automotive Computing: Engineering in Overdrive** - Stanford [\[more\]](#)

July 1- Aug 5: **International Joint Conference on Neural Networks** - Doubletree Hotel, San Jose [\[more\]](#)

August 9-11: **6th Annual Flash Memory Summit** - Santa Clara Convention Center [\[more\]](#)

August 14-19: **IEEE International Symposium on Electromagnetic Compatibility** - Long Beach [\[more\]](#)

Nov 13-17: **37th Int'l Symposium for Testing and Failure Analysis** - San Jose Convention Center [\[more\]](#)

Santa Clara University Grad School of Engineering

Summer "Open University" Classes [\[more\]](#)
- Linear Algebra - Speech Coding - Applied Math
- Intro to Systems Engineering more

Career Development

Professional Skills Courses [\[more\]](#)
- Flexibility: Understanding Differences and Conflict
- Influential Communication - Managing Time and Multiple Priorities - Getting Things Done Across Organizational Borders - Team-Based Accountability -

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IEEE GRID

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for news for technologists, managers and professors, the editorial objectives of IEEE **GRID** are to inform readers of newsworthy IEEE activities sponsored by local IEEE units (Chapters, Affinity Groups) taking place in and around the Bay Area; to publicize locally sponsored conferences and seminars; to publish paid advertising for conferences, workshops, symposia and classes coming to the Bay Area; and advertise services provided by local firms and entrepreneurs.

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NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: www.e-GRID.net



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SCU Summer Open University

Have you ever wanted to continue your education in engineering while you continued working? Santa Clara University's School of Engineering offers graduate degree and non-degree programs to both full-time students and working professionals. Simplified registration for the Summer Open University. Graduate-level instruction. Up to 12 units may be transferred to a graduate-degree program.

Early-morning classes:

- Linear Algebra - Speech Coding - Applied Math - Intro to Systems Engineering (and more)

Evening classes:

- Web Architecture & Protocols - Logic Design Using HDL - IC Fab Processes - Nanoelectronics (and more)

Saturday classes:

- Wireless Mobile Networks - Design of SOCs - Law, Technology, IP (and more)

Prepare for that next project or assignment!

Register today

Students may continue to register until June 5.

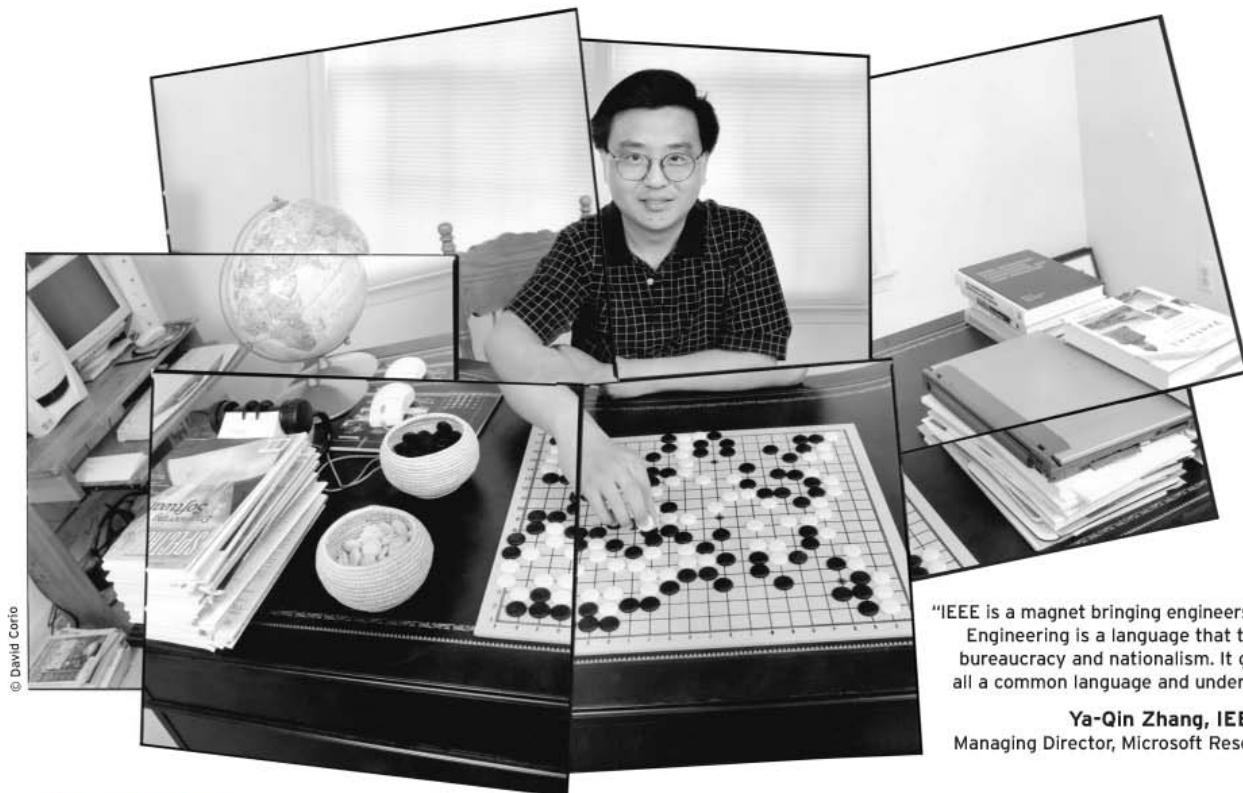
Located in the heart of Silicon Valley, with easy parking.

Choice of three Sessions:

- Session I - 10-week classes (June 13 - August 19)
 - Session II - 5-week classes (June 13 - July 15)
 - Session III - 5-week classes (July 25 - August 26)
- ... plus a number of one-day Saturday classes

Review summer Open University courses:

www.scu.edu/engineering/graduate



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Ya-Qin Zhang, IEEE Fellow
Managing Director, Microsoft Research Asia



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EMC 2011

Long Beach, CA

August 14-19, 2011

Be part of "Harmonizing Waves for EMC" as we step into the future of Electromagnetic Compatibility



IEEE

INTERNATIONAL SYMPOSIUM ON ELECTROMAGNETIC COMPATIBILITY

Long Beach Convention Center

We have planned a diverse range of technical sessions, meetings, experiments, demonstrations, professional development, society awards, and some Special Sessions on EMC in Space – with a wide range of Workshops and Tutorials offering a wealth of information on basic EMC, measurements and testing, reverberation chambers, modeling, electronic vehicles and transportation, standards, and more.

Mr. Henry Ott chairs the Tutorial Session on the Fundamentals of EMC, and Dr. Howard Johnson chairs a Special Session on Signal Integrity. Henry Ott is considered by many to be the nation's leading EMC educator, and has over 40 years experience in the field of EMC. Howard Johnson is a foremost authority on signal integrity, and has over 30 years of experience.

Invited Sessions

• Solving Large EM Problems • Signal Integrity for High Speed Connectors • Full Channel Characterization • EMC in Space (17 papers)

Other events

Computer Modeling & Simulation Demonstrations

Fundamental EMC numerical and computational electromagnetic (CEM) modeling approaches and simulation methods are illustrated through various interactive computer demonstrations.

Hardware Experiments & Demonstrations

Focus on innovative concepts and methods of interest to practicing EMC engineer.

Plus several dozen specialized collateral meetings, receptions.

WORKSHOPS

Some of the titles:

- Fundamentals of EMC
- Fundamentals of Signal Integrity
- Intro to EMI Modeling Techniques
- Application of Reverberation Chambers
- Low Frequency EMC (Power Quality, Energy Efficiency, Electric Vehicles Smart Grid)
- ESD & Lightning Requirements/Testing
- EMC Leadership Training
- Fundamentals of EMC
- EMC Aspects of Smart Grid
- Breaking Down Complex Systems Into Realistic, Solvable Accurate Models
- Transportation System EMC
- Advanced Antenna & Probe Topics
- EMC & Wireless Devices
- EMC Consultant's Toolkit
- Relationships between Transfer Impedance & Shielding Effectiveness
- Predicting Cosite Interference (*and more*)

Hotel at/near the Convention Center:

The Hyatt Regency is located steps from the Long Beach Convention and Entertainment Center. Please reserve by July 15th.

Earlybird Rates through **July 7th**. Special reduced fees for retired/unemployed and for students.

For more information on the **Symposium**, a complete listing of **exhibitors**, and **registration forms**, please visit:

www.emc2011.org

Limited **exhibit space** may still be available; local exhibitors are welcome. Interested exhibitors should contact **Mary Ellen Vegter** at mevegter@threedimensions.com for more information.

IEEE Professional Skills Courses

Managing Time & Multiple Priorities

- Date/Time: Tuesday, July 19, 9:00AM-1:0PM
- With Peter Turla
- Location: Synopsys, Sunnyvale
- Fee: \$300 for IEEE Members; \$350 non-members

Presentation Skills for Engineers

- Date/Time: Friday, July 22, 9 AM – 5 PM
- Location: – Integrated Device Technology, San Jose
- Fee: \$500 for IEEE Members; \$550- non-members

Influential Communication

- Date/Time: Tues, Aug 2, 8:30AM – 4:30PM
- Location: – TIBCO Software, Palo Alto
- Fee: \$400 for IEEE Members; \$500 non-members

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SCV Chapters, Technology Management & Components,
Packaging and Manufacturing Technology Societies

Getting Things Done Across Organizational Borders

- Date/Time: Tuesday, Aug 9, 9:00AM-5:00PM
- Location: Synopsys, Mt. View
- Fee: \$400 for IEEE Members; \$500 non-members

Project Management: Team-Based Accountability

- Date/Time: Thurs-Fri, Aug 18-19, 9 AM – 5 PM
- Location: Integrated Device Technology, San Jose
- Fee: \$625 for IEEE Members; \$700- non-members

For complete course information, schedule, and
registration form, see our website:

www.EffectiveTraining.com*

2011 International Joint Conference on Neural Networks DoubleTree Hotel, San Jose July 31 - August 5, 2011

21 sessions 8 Workshops 20 Tutorials

IJCNN features invited plenary talks by world-renowned speakers in the areas of neural network theory and applications, computational neuroscience, robotics, and distributed intelligence. In addition to regular technical sessions with oral and poster presentations, the conference program includes special sessions, competitions, tutorials and workshops on topics of current interest.

There is a special all-day symposium on Tuesday, Aug. 2, titled "**From Brains to Machines**", featuring invited talks and a panel discussion by leading researchers in neuroscience, cognitive science, cognitive computing and embodied systems.



Sponsored by the
International Neural Network Society (INNS) and
the IEEE Computational Intelligence Society

Plenary Speakers:

Michael Arbib, USC, "**Brains, Machines and Buildings**"
Leon Glass, McGill U, "**Challenges for Computational
Vision: From Random Dots to Wagon Wheel Illusion**"
Dharmendra Modha, IBM, "**Cognitive Computing:
Neuroscience, Supercomputing, Nanotechnology**"
Andrew Ng, Stanford, "**Unsupervised Feature Learning
and Deep Learning**"
Stefan Schaal, USC, "**Learning Motor Skills in Humans
and Humanoids**"

Post-Conference Workshops (Aug. 4, 5)

Future Perspectives of Neuromorphic Memristor Science &
Technology - Problems and Challenges Mapping Spiking
Neurons to Cognition and Behavior - Concept Drift and
Learning in Nonstationary Environments - Cognition and
the Fringe: Intuition, Feelings of Knowing, and Coherence
- Integral Biomathics - Results & Methods of the Neural
Network Grand Forecasting Challenge on Time Series
Prediction - Neuromorphic Hardware: VLSI Spiking
Neural Networks (SNN) and Bio-Sensors

Save, through July 7th

www.ijcnn2011.org



6th Annual Flash Memory Summit

August 9-11, 2011

Santa Clara Convention Center
Santa Clara, CA

FLASH: A Key Technology Enabling New Designs at the only conference dedicated to flash memory!

Flash memory is a key technology enabling new designs for many products in the consumer, computer and enterprise markets. The **Flash Memory Summit** is the only place where you will hear the people who are making these products happen! Network with companies and people that will create the next generation of hardware and software.

This important three-day event will be packed full of tutorials, in-depth sessions and ten keynotes from industry experts.. Get the latest from leaders in the field on: Flash in computers and enterprise, cards and SSDs, flash controllers, improvements in storage capacity and reliability, designing with flash memory, new non-volatile storage technologies, *Customer Talks Back* session, and more!



Topics of Interest

- Design methods
- Flash software
- Flash controllers
- Consumer applications
- Embedded applications
- Standards
- Programming methods
- Hybrid systems (disk or DRAM)
- Interoperability
- Testing
- Flash disks
- Memory cards
- Other non-volatile technologies
- Computer applications
- Power consumption

Participating Companies include Intel, Micron, SanDisk, Spansion, MOSAID and many more.

Who Should Attend?

- Designers of hardware, software, consumer electronics, memory and embedded systems
- Applications, storage, communications, computer, systems, and test engineers
- Storage specialists
- Engineering managers, systems analysts, solution providers and consultants
- VARs, OEMs, system integrators, venture capitalists, marketing and product managers



Pre-Conference Workshop: "Flash Security"

Keynote Speakers

- Glen Hawk, Micron
- Eric Kao, Memoright
- Sanjay Mehrotra, SanDisk
- Knut Grinsrud, Intel
- John Scaramuzzo, SMART Modular
- Scott Stetzer, STEC ... and more

Earlybird rates through **August 6**

For more information, and to register online:

flashmemorysummit.com

Save \$100 – use Registration Code "**IEEE**"

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TUESDAY July 12, 2011

Future Vehicle Computer System in a Five-Screen World

Speaker: Roger D. Melen, Senior Advisor, Toyota InfoTechnology Center U.S.A., Inc.
Time: Networking and light dinner at 6:30 PM; Presentation at 7:00 PM
Cost: \$2 donation accepted for food & drinks
Place: Cadence Bldg 10, 2655 Seely Ave, San Jose
RSVP: from the website
Web: sites.ieee.org/scv-cs

Roger D. Melen has been a Senior Advisor at Toyota InfoTechnology Center U.S.A., Inc. for past eleven years, providing advice related to the deployment of advanced computer and networking technologies in future vehicle designs. He has worked as Vice President R&D of Canon Research Center America for eleven years on the deployment of networked computers in CMOS office and photographic imaging systems. Prior that that he was a founder of Cromemco Inc. an early and dynamic microcomputer company. In his early work he pioneered CCD image sensors in his PhD research at Stanford University in 1973 and while in industry has applied for 60 patents. He authored the widely respected IEEE book: **CCD Technology and Applications**. He also founded and taught the Electrical Engineering class on entrepreneurship for the past 35 years at Stanford University.

Byron Shaw, PhD, is Managing Director of GM's Advanced Technology Office in Silicon Valley. He has dual roles reporting to GM Global R&D and GM Ventures. He began his career in the automotive industry as a GM Scholar with GM's Harrison Division (Delphi), before a stint as a visiting scientist with Daimler Benz research labs in Stuttgart, Germany. Byron was instrumental in developing the charter of BMW's Technology Office in Palo Alto, where he was the Manager of Advanced Technology and technical director of a 30-person engineering and marketing team and a \$4 million budget where he oversaw the discovery and implementation of new and advanced technologies into BMW's vehicle development process. After leaving BMW, Byron was the co-founder and CTO of a Photovoltaic Solar startup where he led the development team in releasing its first product launch and participated in venture fundraising. *(continued ...)*

Future automobiles will widely incorporate new dashboard display screens which will soon join laptops, cellphones, televisions, and tablets as part of the common fabric of the modern networked world. They will incorporate images and data to provide information, entertainment, communication, and driving assistance in the vehicle cabin as well exchange data with electrical and hybrid powered drivetrains and their battery power systems. Smartphones are being integrated with vehicle electronics to provide a seamless computing fabric for both drivers and passengers. In contrast with other computers, vehicle considerations for safety dominate over decisions for the other important design factors such as performance, value, fun and security. The abilities and psychology of the driver behavior are important in achieving overall system improvement.



Byron has consulted for several high-tech Silicon Valley companies in the electronics and software industries and is a founding board member of SmallTech LLC. Byron holds BS and MS degrees in Mechanical Engineering and a BS in German Language and Literature from MIT. His PhD was completed at the University of California at Berkeley in the Vehicle Dynamics and Control Laboratory, focusing on engine emissions modeling and control, embedded electronics and digital signal processing.

WEDNESDAY July 13, 2011

Networked Control Systems II: Innovative Topologies for Distributed Motion Control

Speaker: Jason Goerges, ACS Motion Control, Inc.
Time: Pizza and networking at 6:30 PM;
Presentation at 7:00 PM
Cost: none
Place: Cogswell Polytechnical College, Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/css

Jason Goerges is a native of Minnesota, and received his Bachelor's Degree in Electrical Engineering and Minor in Business Management from the University of Minnesota. He went on to receive a Master's Degree in Electrical Engineering from Arizona State University with a focus on digital signal processing and control systems. After working as an engineer at Honeywell Flight Control Systems, Jason joined ACS Motion Control in 2007 and currently resides near Minneapolis with his wife. He enjoys spending time with family and friends, and being active in his local community.

With a modern industrial ethernet network like EtherCAT, it is now possible to provide fully coordinated real time multi-axis motion control with a distributed architecture. Traditionally, achieving this level of performance was best handled with a centralized architecture because of the required bandwidth and deterministic communication. If the features of a modern real-time industrial ethernet network like EtherCAT is used, the performance of a centralized controller can be extended to a network based approach, which has many benefits (scalability, low cost, easy connectivity).



WEDNESDAY July 13, 2011

Architectures and Signal Integrity Challenges for 100 Gbps Data Transmission Systems

Speaker: Lux Joshi, Product Specialist, LeCroy Corporation
Time: Food and networking at 6:00 PM; Presentation at 6:30 PM
Cost: \$5 donation is requested for refreshments
Place: National Semiconductor Auditorium (Bldg E), 2900 Semiconductor Drive, Santa Clara
RSVP: from website
Web: www.ewh.ieee.org/r6/scv/comsoc

Lux Joshi is a Product Specialist at LeCroy Corporation supporting business development for the WaveMaster 8Zi oscilloscope product line for high speed serial data analysis and signal integrity applications. He holds a BS from Columbia University and an MS from Stanford University both in Electrical Engineering. Lux previously worked in various capacities at LeCroy including R&D and marketing and holds multiple patents for oscilloscope hardware and software.

100 Gbps networks are being developed to address the need for substantially higher bandwidth in core networking applications. However, there are technical hurdles in implementing end-to-end 100Gbps transmission systems which require advances in all elements of the ecosystem - from more sophisticated SERDES to higher order modulation formats.

This talk will give an overview of architectures for 100Gbps systems (in both deployed and proposed systems). In addition standards work around these systems will be presented, including IEEE 802.3 variants as well as OIF CEI-28G standards. Channel models and transmit/receive topologies will be described. Jitter measurement and SI validation techniques for 25+Gb lanes will be addressed. Finally, system performance will be discussed.

Background: Next generation electrical components, interfaces, and channels for these systems are challenging to implement and deploy. Current implementations for 100Gbps systems distribute 10Gbps electrical links across 10 separate paths (or "lanes") to interface to the Physical Medium Dependent sublayer (PMD). However, such wide interfaces can be costly in terms of power and size. Coherent modulation schemes, such as DP-QPSK, have been proposed to transmit 100G baud data streams over existing optical fiber infrastructure which rely on complex modulation of 4 x 25 Gbps streams. Consequently, a logical choice of electrical interface for this system would be a 4 x 25Gbps architecture which would necessitate electrical components (chips, PCBs, connectors, etc.) transmit and process the data in real-time.

The common challenge among the multitude of approaches in implementing electrical interfaces of 100Gbps systems is signal integrity. As lane rates increase from 10 Gb/s to 25+Gbps, Physical layer signal integrity at these speeds need to be carefully managed in order to guarantee link performance and interoperability. Channel modeling and equalization become increasing complex issues. Furthermore, crosstalk and spurious aggressors coupling onto high speed lines can become dominant jitter sources causing degraded link performance if not managed properly. We will address all these critical issues and more in this talk.



THURSDAY July 14, 2011


Power System Reliability Analysis and Artificial Intelligence

Speaker: Zach Cramer, Pacific Gas and Electric Co.
Time: Food and networking at 12:00 PM; Presentation at 12:15 PM
Cost: Free for IEEE members, \$5 for non-members
Place: CA Public Utilities Commission, Golden Gate Training Room, 505 Van Ness Ave, San Francisco
RSVP: by July 12 to John Joven, JRJJ@pge.com 415-973-4873
Web: www.e-grid.net/docs/1107-sf-pes.pdf

Zach Cramer works for Pacific Gas and Electric Company as an electric transmission planning engineer for California's San Joaquin Valley. Pacific Gas and Electric Company is headquartered in San Francisco, and provides gas and electric service for most of Northern California. He has also worked with PG&E's distribution planning and reliability engineering departments and with the CAISO's renewable integration team. He received his Bachelors of Science in Electrical Engineering from California State University, Sacramento in June, 2009.

In the early 1990's many utilities chose a strategy of maximizing return on equity. Under this strategy very little capital investment was made, leading to increased asset utilization and decreased contingency reserves. At the same time much of the existing infrastructure was nearing end of life. As a result, customer reliability was severely degraded. When it became apparent that such poor reliability isn't economically attractive to service providers or their customers, utilities began aggressive reliability improvement programs. Unfortunately, many utilities lacked the expertise required to manage these programs effectively.

The goal of this presentation is to communicate the information necessary for the implementation of a successful reliability engineering program. The will be a focus on two topics: 1) a simple organized approach for computing the cost of customer reliability, and 2) discussing how techniques from artificial intelligence can be applied to improve power system planning and operations. Part 1 will cover reliability analysis in detail and will have several transmission reliability examples. A substation reliability decision matrix will also be presented. Part 2 will be more of a high level discussion of popular artificial intelligence techniques and how they can be applied to reliability engineering. This section will also have some interactive demonstrations.



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SATURDAY July 16, 2011

**One-day Seminar: Emerging
Automotive Computing:
Engineering in Overdrive**

Keynote: Dr. Steve Shladover, PATH (Partners for Advanced Transportation Technology), UC Berkeley Inst of Transportation Studies
Time: Registration at 8:30 AM; program from 9:00 AM - 4:30 PM
Cost: See website after June 5th (approx \$50 fee)
Place: Braun Auditorium, Stanford University, Stanford
RSVP: from website
Web: sites.google.com/a/nfic-us.org/nfic-2011

For details about speakers, registration, please see the Chapter's website.

**Int'l Joint Conference on
Neural Networks**

July 31 - Aug 5, 2011
DoubleTree Hotel, San Jose

- 20 Tutorials - 32 Special Sessions
- 8 Workshops - Regular Sessions

Focus on Autonomous learning,
theory & models, Brain-machine
interfaces, Autonomous learning,
Artificial Life ... more

Save, through June 30

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Email: Dave.Stevens@StevensLawGroup.com

TUESDAY July 19, 2011

A Breakthrough in Nanocomposite for High-Capacity Hydrogen Storage

Speaker: Jeff Urban, Molecular Foundry

Time: Registration & light lunch 11:30 AM;
Presentation at 12:00 PM

Cost: Members and Students \$5. Non-Members
\$10

Place: National Semiconductor Bldg E-1 CMA
Room. 2900 Semiconductor Drive, Santa
Clara

RSVP: from website

Web: www.ieee.org/nano

Berkeley Lab researchers have designed a new composite material for hydrogen storage consisting of nanoparticles of magnesium metal sprinkled through a polymer related to Plexiglas that rapidly absorbs and releases hydrogen at modest temperatures without oxidizing the metal after cycling. This achievement is a major breakthrough in materials design for hydrogen storage, batteries and fuel cells.

Dr. Jeff Urban is Deputy Director of the Inorganic Nanostructures Facility at the Molecular Foundry, a DOE Office of Science nanoscience center and national user facility located at Berkeley Lab. Dr. Urban has a Ph.D. in Physical Chemistry from Harvard University, presented his work at the Hydrogen Storage and Production Conference, Netherlands, conducted Studies in Synthesis and Measurements of Nanocrystal Transistors, Thermoelectrics, and Photovoltaics, published 32 papers and numerous patents embodying nanotechnology.

WEDNESDAY July 20, 2011

Cyber Security in the Electric Utility Sector (First in a 6-part series)

Speaker: Dan Skaar, Midwest Reliability Organization

Time: 11:00 AM - Noon (first of a 6-part monthly series)

Cost: IEEE Members: \$19 for individual webinar; \$89 for series. Non-Members: \$38 for individual webinar; \$189 for series

Place: via the internet

RSVP: from website

Web: www.ieeeusa.org/careers/webinars/2011/Risk-Management.html

IEEE-USA members will secure the following benefits from these webinars:

- Understand risk management standards, practices, concepts and tools
- Learn about current and emerging career opportunities in cybersecurity, power grid, controls and other areas
- Enhance career options by discussing emerging career opportunities with risk and CIP experts.

IEEE-USA Webinar Series on Risk Management

Recent events have highlighted the importance of risk-based decision-making. Modern systems are becoming more complex; and the economic, safety, and other consequences of a system failure, more serious. Volatility, uncertainty, complexity and ambiguity (VUCA) are challenging all organizations and all engineers. Ignoring risks, because they are improbable or not worth analysis, has proven to be highly risky in itself. Managing the risks of disruptive events is becoming a critical focus for business and society. For example, the need for security to mitigate electric reliability risks has been formalized as a regulatory requirement, by the North American Electric Reliability Corporation (NERC) known as Critical Infrastructure Protection (CIP).

This webinar series focuses on risk-based, problem-solving and decision-making, and the application of risk management standards and practices for public safety and Critical Infrastructure Protection (CIP).

The objective is to provide relevant and directly applicable information that technology and operational professionals can use in their jobs, and to enhance their long-term employability.

Risk management represents new work/career/job engineering opportunities:

- Opportunities in security implementation and evaluation for key areas of the electric power industry
- CIP, cybersecurity, cyber-physical systems, controls (SCADA), Smart Grid, etc.
- Driven by U.S. statutes and federal regulations -- work (jobs) won't disappear
- High barriers to entry -- requires technical/engineering expertise
- Won't be outsourced:
 - Public safety, domestic security work
 - High tech, high touch
 - National security
- Good/great pay - Low supply and high technical demand

WEDNESDAY July 20, 2011

Design and Implementation of Ethernet Magnetics and Power Magnetics using Planar PCB-Based Embedded Ferrite Technology

Speaker: Dr. Sidharth Dalmia, Senior Manager, Development Engineering, TE Connectivity
Time: Networking & Pizza at 6:00 PM; Presentation at 6:30 PM
Cost: none
Place: National Semiconductor Building E Auditorium 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/pels

Dr. Sidharth Dalmia is currently a Senior Manager for Development Engineering at TE Connectivity (formerly Tyco Electronics). In this role he is primarily responsible for development of Planarmag products.

Previously, Sidharth was the Vice President of Engineering for Planarmag Inc., as well as the Director and Co-founder of Jacket Micro Devices (JMD) Inc. JMD and Planarmag have been pioneers in the use of laminate-based technology with embedded passives including ferrites, discrete and modules. Planarmag was acquired by Tyco Electronics Corporation and JMD was acquired by AVX Corporation.

Sidharth has co-authored more than 100 IEEE and IMAPS journals and conference papers. He holds nine US patents and several international patents with more than 20 US and international patents pending. Sidharth's work has won him best IEEE Transactions and IEEE Conference paper awards from the IEEE CPMT society. His doctoral thesis was nominated for the Georgia Institute of Technology outstanding thesis of the year award in 2002.

Sidharth received his Bachelor of Science, Masters of Science and Doctoral in Electrical Engineering from Georgia Institute of Technology in 1998, 1999 and 2002 respectively and has held several faculty positions at the institute.

Miniaturization, increased throughput and functionality are key drivers in the deployment of Ethernet switches/routers, mobile handheld devices and laptops. Isolation transformers, common mode chokes, power chokes and power inductors are key components used in these applications. This presentation presents a novel multilayer PCB-based substrate technology for such components that provides for large economies of scale and a lower cost alternative to hand-wound or machine-wound devices.

The presentation will show novel design, implementation, measurements, reliability data and integration of multiple ferrite components such as 1:1 Ethernet transformers for IEEE 802.3 at electromagnetic interference (EMI) chokes, 4 Amp to 6 Amp power EMI chokes for laptops, and 1 Amp to 25 Amp power inductors for laptops. These components and process technologies are being targeted as a cost-effective, high-performance, miniaturized alternative to hand-wound and machine-wound technologies.

The first example of this technology is 10/100 discrete magnetics, which integrate the required magnetics for two Ethernet channels. These components can be mounted on either side of a host PCB using lead-free reflow processes with a thousand components manufacturable on one PCB. Each of the two channels consists of a 1:1 transformer with an open circuit inductance of 500 uH at 100 KHz while meeting an isolation voltage of 2250V DC. These transformers are constructed based on cross-section and design rules that allow for a pair of 100 Ohm differential lines to be wrapped around the ferrite with tight precision. The metal layers are connected from top to bottom using differential through vias. The spacing/line width of the differential lines are uniquely chosen so that they can provide 2250V isolation while providing stable impedance over 100 KHz to multi-GHz. Chokes are mounted on the top side of transformers and can also be embedded in the substrate. A combination of these transformers and chokes are placed in integrated connector modules (ICMs). Finally, this technology is also capable of integrating power inductors and power chokes for DC-Dc applications.

WEDNESDAY July 20, 2011

From Factory to Field: Developing Utility-Scale PV Projects

Speaker: Glen Davis, CEO and Co-Founder, Agile Energy, Inc.

Time: Networking at 6:30 PM; Presentation at 7:00 PM

Cost: none

Place: Palo Alto Research Center (G.E. Pake Auditorium), 3333 Coyote Hill Road, Palo Alto

RSVP: not required

Web: www.svpvs.org

Mr. Davis will discuss what's required to transform solar equipment coming off the assembly line into a large operating power plant. He will also explore the various types of companies competing to develop utility-scale PV projects, the landscape on which they compete, and where the PV project development business is headed.

Glen Davis is the Chief Executive Officer and a Co-Founder of Agile Energy, Inc. Headquartered in San Bruno and financially backed by Good Energies, Inc. since December 2009, Agile Energy develops utility-scale electric power generation assets in North America, primarily deploying solar photovoltaic and concentrated PV technologies. The company currently has over 500 MW of projects in its pipeline.

Mr. Davis spent the first 18 years of his energy career with the AES Corporation, helping build it into one of the leading global independent power producers. At AES, he led the development, financing, acquisition, and sale of power generating assets on four continents, worth billions of dollars.

In March 2004, Mr. Davis co-founded Agile Energy LLC with Rob Morgan, providing development and consulting services to the independent power industry. Today's company, Agile Energy, Inc., builds upon the foundation and track record established by Agile Energy LLC. Mr. Davis served as Executive Vice President and Chief Commercial Officer for Ausra, Inc. from 2007 to 2008.

Mr. Davis served on the Board of Trustees of the Western Systems Coordinating Council from 1998 through 2002. He holds an MBA from the Massachusetts Institute of Technology and a Sc.B. in Mechanical Engineering from Brown University.

WEDNESDAY July 20, 2011

**Tour of 300kW PV
Solar Tracking System**

Speakers: Steve Birndorf, Project Developer, and
Gary Buchanan, Project Manager,
Borrego Solar Systems, Inc.

Time: Social/Snacks/Drinks at 5:30 PM;
Presentation and tour at 6:00 PM

Cost: none

Place: Del Valle Water Treatment Plant, 601
Vallecitos Road, Livermore

RSVP: for first 30, by email to Henry Chan,
Henry@EDesignC.com

Web: ww.ewh.ieee.org/r6/oeb/ias.html

THURSDAY July 21, 2011

Intellectual Property Traps and Opportunities for Employed Future Entrepreneurs

Speaker: Orin E. Laney, former chair of the IEEE-USA Intellectual Property Committee

Time: 6:30 PM

Cost: none

Place: KeyPoint Credit Union, 2805 Bowers Avenue, Santa Clara

RSVP: from website

Web: ieescvpacejuly2011.eventbrite.com

Orin E. Laney, BSEE, MBA, PE, NCE, SM-IEEE is a member and former chair of the IEEE-USA Intellectual Property Committee. As a design engineer at both large and small companies, and as a business owner and employer he has experienced the issues to be discussed from both sides of the table. Mr. Laney is an entertaining National Speaker on behalf of the IEEE, and has spoken pro bono at over 100 college campuses and section meetings on intellectual property rights, starting a business, career management and similar professional matters.

This is not a talk on patents and copyrights, but goes far beyond such things. The focus is on the division of intellectual property rights between yourself as a creative person and those you perform labor for, whether as an employee, consultant, or independent creative person.

Every schematic, code listing, and disclosure has intellectual property rights that automatically attach upon creation. The way you handle these will determine your legal standing to own and exploit the fruits of your labor – or not – depending on what you sign and the actions you take. The core of this talk is an eye-opening career strategy for protection of personal intellectual property. Key intellectual property opportunities and pitfalls will be discussed.

Case histories – some of them hair-raising — will be used to underscore salient points. This is a must-hear talk for anyone with aspirations beyond toiling for a salary, especially those with entrepreneurial plans. Even if you simply want to pursue a hobby in a technical field, there are lessons that can help you avoid unexpected intellectual property tar pits.

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TUESDAY July 26, 2011

Tour: SMT (Surface Mount Technology) Manufacturing and Engineering

Speaker: Affif Siddique, VP - Strategy & Business, Whizz Systems, and staff
Time: Intro at 4:00 PM; small-group tours from 4:15 - 6:15 PM; pizza and drinks at 6:00 PM
Cost: none
Place: Whizz Systems, Inc, 3240 Scott Blvd, Santa Clara
RSVP: from website
Web: tourwhizzsystems.eventbrite.com

On July 26th, Whizz Systems and its senior staff will host an Open House for IEEE CPMT and ComSoc chapter members and their guests. Attendees from other IEEE Societies and Alliance organizations who are interested are also welcome to attend. We will offer a brief introduction to Whizz Systems and information-packed tours of our SMT (Surface Mount Technology) Manufacturing and Engineering design plant.

Tour participants will learn how the complete PCB (Printed Circuit Board) design and assembly process works today (which is quite different from what was done several years ago). They will experience an inside view of a complete design and manufacturing facility, learn about ISO best practices, how ESD and different packaging issues get handled in a state of the art product design and manufacturing environment.

Attendees will be able to interact with our Engineering Design and Product Development teams. We will reveal what product engineering tools are being used and how our teams select different approaches for different products and design methodologies. We'll describe how original BGA (Ball Grid Array) work [as well as BGA re-work] is done and how it's tested on 3DX, 5DX and AOI (Automated Optical Inspection) machines.

In summary, we'll demonstrate the complete product engineering and manufacturing process from BOM (Bill of Material) procurement to finished product assembly on SMT machines. Attendees will also learn how feeders work, the difference between Lead base and RoHS (Restriction of Hazardous Substance or Lead-Free), testing and other technical issues.

If you are interested in packaging, contemporary product engineering design, assembly and/or state of the art manufacturing processes, this tour is for you!

Schedule:

4:00 - 4:15pm Registration and Introduction from Whizz Systems Staff
4:15pm - 6:15PM Continuous tours in separate, small groups
6:00 - 7:00PM: Networking, Pizza, Snacks, Soft Drinks



- Multiphysics, Multidisciplinary Engng
- CFD, Stress, Heat Transfer, Fracture
- Fatigue, Creep, Electromagnetics
- Linear/Nonlinear Finite Element Analyses
- Multi-objective Design Optimization
- BGA Reliability

Ozen Engineering (408) 732-4665
info@ozeninc.com www.ozeninc.com

WEDNESDAY July 27, 2011

Nanofabrication of Bit-patterned Media by Block Copolymer Directed Assembly

Speaker: Ricardo Ruiz, Hitachi GST
Time: 3:00 PM
Cost: none
Place: Lawrence Berkeley National Labs
RSVP: required, by email to Kate Jenkins, cajenkins@lbl.gov
Web: ewh.ieee.org/r6/oeb/mag

Dr. Ricardo Ruiz received his PhD in Physics from Vanderbilt University where he worked on thin film growth of organic electronic materials. He was a postdoctoral fellow at Cornell University where he explored the correlations between structural and electronic properties of pentacene thin film transistors. In 2004 he joined IBM T.J. Watson as a postdoctoral fellow where he learned about block copolymer self assembly and its applications for high density lithography. In 2006 he became a research staff member at Hitachi GST where he works on template nanofabrication for bit patterned media technology using block copolymer self assembly



Block copolymer directed self assembly continues to make advances that place this technology as a potential candidate for sub-20nm lithography. The naturally periodic features found in block copolymer films display superior size uniformity at ultra-high densities, making them ideal lithographic masks to define the highly periodic data bits in the data sectors of hard disk drives for bit patterned media (BPM) technology at densities beyond 1Tbit/in². Nanofabrication challenges in magnetic BPM, however, reach far beyond pattern formation. I will review recent progress at Hitachi GST in all aspects involving template nanofabrication by directed assembly. These include control over feature size uniformity, bit shape, placement accuracy, metrology, distorted lattices on circular tracks, high fidelity pattern transfer, magnetic BPM fabrication, impact of bit size uniformity on the magnetic switching field distribution and, more recently, the fabrication of rectangular bits in a rectangular lattice. In all these aspects, the high uniformity of block copolymer patterns outperforms that of e-beam lithography alone bringing an exciting opportunity for self-assembly in time for bit patterned media technology.

WEDNESDAY September 28, 2011

The Role of Information Theory in Public Key Cryptography

Speaker: Dr. Martin E. Hellman, Professor Emeritus
of Electrical Engineering, Stanford University

Time: Refreshments at 5:30 PM; Presentation at
6:00 PM

Cost: none

Place: 202 Packard Bldg, Stanford University,
Stanford

RSVP: not required

Info: Art Astrin, art_astrin@yahoo.com

Prof. Martin E. Hellman received his B.E. from New York University in 1966, and his M.S. and Ph.D. from Stanford University in 1967 and 1969, all in Electrical Engineering.

Prof. Hellman was at IBM's Watson Research Center from 1968-69 and an Assistant Professor of EE at MIT from 1969-71. Returning to Stanford in 1971, he served on the regular faculty until becoming Professor Emeritus in 1996. He has authored over seventy technical papers, six US patents and a number of foreign equivalents.

Hellman is best known for his invention, with Diffie and Merkle, of public key cryptography. In addition to many other uses, this technology forms the basis for secure transactions on the Internet. He has also been a long-time contributor to the computer privacy debate, starting with the issue of DES key size in 1975 and culminating with service (1994-96) on the National Research Council's Committee to Study National Cryptographic Policy, whose main recommendations have since been implemented.

People are often surprised that public key cryptography was invented within Stanford's EE department, not the Computer Science department. Yet my background in Information Theory played a key role in that advance. This talk reviews my professional odyssey, from research in more traditional information theory to cryptography to estimating the odds that civilization will survive another century. The unifying theme is the role that my training in information theory played in guiding that journey.

