CHAPTER MEETINGS

SCV-Phot - 9/6 | **Photonic Technologies for Datacenter Networking** - mega-datacenters, architecture, scaling, photonic interconnects ... [more]

OEB-Mag - 9/7 | **Magnetic Soft X-Ray Microscopy: Imaging Magnetism Down to Fundamental Length and Time Scales** ... [more]

SCV-Life - 9/12 | **California Water: Crisis or Crossroads?** - polarizing issue, farms vs. cities, vital resource, changes ... [more]

SCV-CS+SPS - 9/13 | **GPU Computing: Taming a 23,000-Thread Beast!** - as supercomputers, history, evolution, challenges ... [more]

SCV-EMC - 9/13 | **Designing PCB Stackups to Balance Signal Integrity Against Manufacturability** - rules, targets, stackup ... [more]

SCV-EDS+Nano - 9/13 | **Metal Interconnects for Large-area Power Devices: Physics, Challenges, and Solutions** - typical mistakes ...[more]

SCV-ComSoc - 9/14 | **Telemedicine: New Technologies and Perspectives from the Field** - 3 speakers: exams, streaming … [more]

SCV-CPMT - 9/14 | **fcCuBE Technology: Expanding the Flip Chip Packaging Landscape** - Cu column, , escape routing, stresses ... [more]

SF-ComSoc - 9/14 | **Radio-Access LTE-Advanced and Beyond** - 4G, components, data rates, multi-antenna, relaying, aggregation ... [more]

SCV-PV - 9/14 | **The Consumerization of Energy** - costs, security, imported fuels, climate change, lessons for solar ... [more]

OEB-IAS - 9/15 | **Technology Update: Lighting Controls in Commercial and Industrial Applications** - trends, options, metering ... [more]

SCV-CNSV - 9/20 | IP **Strategies for the New Decade** - IP licensing program, Major players, monetization paths ... [more]

SCV-Nano - 9/20 | **Transfer-Printing Semiconductor Nanodevices on Arbitrary Substrates** - single crystal, top-down, bottom-up ... [more]

SCV-PELS - 9/21 | **Better Place – The Storage Story for Vehicles** - charging infrastructure, storage asset, utility-scale storage ... [more]

SCV-PES+IAS - 9/21 | **Electric Vehicle (EV) Technology & Tour of KLEENSPEED Technologies** - functionality, viability, potential [more]

SCV-CPMT - 9/22 | **Memory Scaling and Its Potential Impact on Computing and Storage** -, hierarchies, impacts, packaging ... [more]

SCV-CAS - 9/26 | **Video Compression Technology – Building the Next Generation** - resolution, perceptual quality, high-def ... [more]

SCV-IT - 9/28 | **The Role of Information Theory in Public Key Cryptography** - research, theory, preparation, training ... [more]

SCV-Phot - 10/4 | **Green Photonics Trends for the Next Decade: Communications, Lighting, Solar** - rare earth oxides, solutions . [more]

SCV-TMC - 10/6 | **Product Management for Project and Program Managers** – good/bad experiences, roles, better cooperation ... [more]

SCV-CPMT - 10/12 | **Silicon Carbide (SiC) Sensing Technology for Extreme Harsh Environments** - growth, metallization ... [more]

SCV-CNSV - 10/18 | **Leveraging Consulting to Build a Bionic Technology Company** - iterations, prototypes, validation ... [more]

SCV-Rel - 10/21 | **Quality: On the Road to Performance Excellence** - 1-day seminar: over 20 talks in 5 tracks, reception ... [more]

Conference Calendar

Sept 19-20: **Chip-Packaging Co-Design for High Performance Electronic Systems** - Santa Clara [more]

Sept 26-29: **Online Conference on Energy-Efficient Comm'ns & Green Technologies** - on Internet [more]

Oct 16-20: **Frontiers in Optics '11, with Laser Science XXVII** - Fairmont Hotel, SJ [more]

Nov 6-9: **Android Developer Conference (AnDevCon)** - Hyatt Regency Burlingame [more]

Nov 13-17: **37th Int'l Symposium for Testing and Failure Analysis** - San Jose Convention Center [more]

Nov 29 - Dec 2: **Printed Electronics USA Conference** - Santa Clara Convention Center [more]

CALLS FOR PAPERS:

March 19-21: **International Symposium on Quality Electronic Design** - Techmart, Santa Clara [more]
- Abstracts Due **Sept. 29th**

March 19-20: **Engineering Design Education Conference** - Techmart, Santa Clara [more]
- Abstracts Due **Sept. 29th**

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From the Editor

Last weekend was IEEE's Sections Congress, in San Francisco. Thanks, Tom Coughlin (also Roger Hoyt, Allen Earman, Ed Aoki and Dick Ahrons) for planning and conducting this event, and the CHM Open House! SC is held every three years, in one of the word's major cities. Present were the Section Chairs from about 300 Sections – Saudi Arabia, Australia, Spain, Brazil, and many more. Joining us were 40^{+} of the IEEE's staff from Piscataway, Washington DC, Los Alamitos, and other places.

I attended as a presentor – giving a Breakout Session on Sunday to about 75 people on the topic of "**Generating Income and Improving Communications Within Your Local Section -- for Medium to Large Sections**". I wanted to give other Sections the "formula" for doing what I've developed here for the **GRID**. Already I've heard from the L.A. Council, the Boston Section,and several others.

Our Council (and the **GRID**) are in a unique position. Rather than being a struggling part of IEEE, our 3 Sections are prosperous and blessed with resources. We also have the largest technical concentration on the planet. Our "problems" are on the "large" side – some of our Chapters are maxed-out as far as being able to deliver program to our members; after all, there are only 12 months in a year. So our solutions sometimes need to be different.

For example, we already have VERY active Chapters for PELS, EDS, CPMT and Photonics – but the SCV Section has voted to form an additional chapter for Photovoltaics, to jointly cover this field for these four groups. This is something the IEEE has never faced, so there isn't a current solution. During Sections Congress, I was able to have a breakfast meeting with Mary Ward-Callan (Managing Director for Technical Activities), Donna Hudson (IEEE's Technical VP) and Celia Desmond (IEEE Canada Past President, IEEE Board member). We figured out a solution, and I'll now work with our MGA people to implement it, for this new Chapter.

There's no replacement for face-to-face meetings, although email (and other methods) can also prove helpful.

Paul

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

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Paper Submission Deadline: Sept. 29, 2011
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Final Camera-Ready paper: January 10, 2012

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- **IP Design, quality, interoperability and reuse**
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- **EDA Methodologies, Tools, Flows**
- **Design for Manufacturability/Yield & Quality**
- **Effects of Technology on IC Design, Performance, Reliability, and Yield**

Submission of Papers

The guidelines for the final paper format are provided on the conference web site. Paper submission must be done on-line through the conference web site at **www.isqed.org**. In case of any problems email isqed2012@isqed.org. ISQED papers are published in IEEE Xplore.

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Interdisciplinary Engineering Design Education Conference

March 19-20 , 2012

Techmart Center, Santa Clara, CA, USA

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Acceptance Notifications: November 24, 2011
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Printed Electronics USA gives the big picture, not least by inviting leading speakers from around the world from a range of industries including consumer goods, healthcare, military, electronics, advertising, publishing and others. Commercialization and the full range of technologies are the emphasis, from interactive packaging and promotional posters to sensing fabrics and ultra low cost wireless identification tags.

Photovoltaics USA covers the solar cell sector. All the latest developments in thin film, organic, printed photovoltaics as well as emerging technologies growing alongside the more established ones, such as luminescent concentrators and infrared harvesting.

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Master Classes on Nov 29, Dec 2 – interactive sessions:
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Tradeshow
Over 100 leading companies will be showcasing innovative technologies and commercial applications in the field of printed electronics and photovoltaics. This is the world's biggest tradeshow on the topic and an ideal place to meet your suppliers, customers and partners in one place. Participate in **Demonstration Street,** featuring examples of printed electronics in action.

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- Date/Time: Th/Fri, Oct 13-14, 9:00AM – 5:00PM
- Location: – TIBCO Software, Palo Alto
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-Sales Operations Supervisor, @Road

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- Date/Time: Thursday, Oct 20, 8:30AM-4:30PM
- Instructor Andrew Oravets
- Location: Brocade Communications, San Jose
- Fee: $400 for IEEE Members; $500 non-members

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SCV Chapters, Technology Management & Components, Packaging and Manufacturing Technology Societies

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- Date/Time: Thurs, Oct 27, 9 AM – 5 PM
- Location: TIBCO Software, Palo Alto
  Fee: $425 for IEEE Members; $500- non-members

Project Management: Team-Based Accountability - PMI Certified

-- Date/Time: Tues-Wed, Nov 8-9, 9:00AM – 5:00PM
-- Location: TIBCO Software, Palo Alto
-- Fee: $625 for IEEE Members; $700 non-members

Meeting Management

-- Date/Time: Tues-Wed, Nov 8-9, 9:00AM – 1:00PM
-- Location: TIBCO Software, Palo Alto
-- Fee: $350 for IEEE Members; $425 non-members

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Tuesday, November 8th 11:00 am – 6:45 pm
Wednesday, November 9th 10:00 am – 2:30 pm

"This was a great conference! The scope and breadth of classes gave a great opportunity to learn more about Android development in general AND gave the opportunity to network with other people at all levels. It's a great learning place with wonderful people!"
Andrew Mauer, Sr. Project Manager, B-Line Express, Inc.

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"Android Awesomeness!" Chet Haase and Romain Guy, Google
"Developing Consumer Apps in a Really, Really Big Company", David Baldie and Andrew Peret, AmEx

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- Alternative Energy (Photovoltaics, SS Lighting, etc.)
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- FA Process/Case Studies
- MEMS, Discretes and Optoelectronic Device FA
- Packaging- and Assembly-Level FA
- Finding Invisible Defects
- Defect Characterization & Metrology
- Test and Diagnosis
- Circuit Edit (Laser, FIB, etc.)
- Counterfeit Electronics Detection and Mitigation
- Photon-Based Fault Isolation Techniques
- Sample Preparation and Device Deprocessing
- Nanoprobing and Electrical Characterization
- Panel Discussion on 'But How Do You Find an "Invisible" Defect?'
- Posters

9 TUTORIALS Sunday & Monday, Nov 13-14

Continuously updated tutorial sessions with new and cutting-edge topics related to failure analysis. **Two New Tutorials This Year!**

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- Fault Isolation
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- Differentiating EOS/ESD

2011 Keynote Address

Dr. Joseph Michael from Sandia
tools and analysis used to identify the origins of the anthrax spores – A MUST ATTEND!

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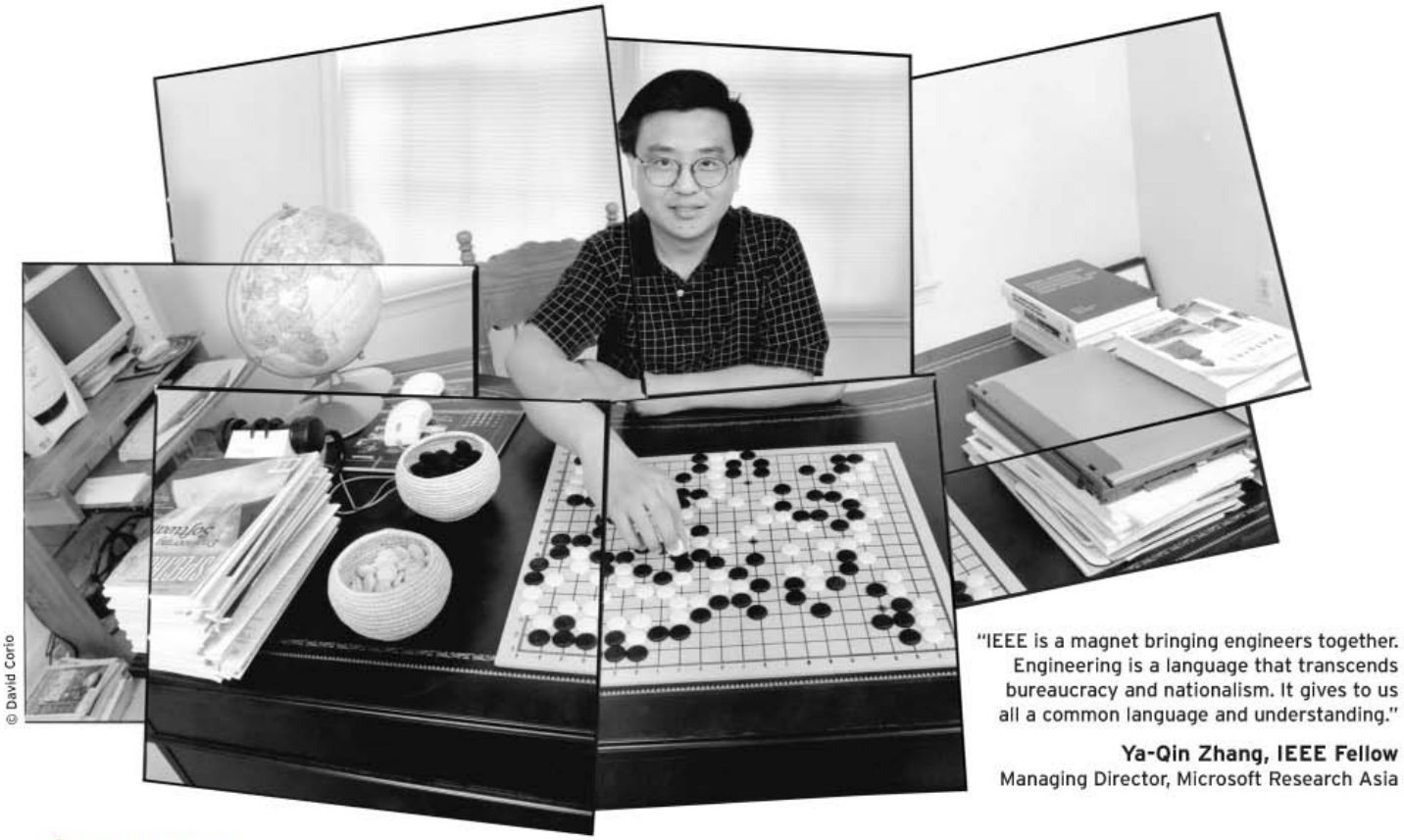

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Ya-Qin Zhang, IEEE Fellow
Managing Director, Microsoft Research Asia

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SCV Photonics

TUESDAY September 6, 2011

Photonic Technologies for Datacenter Networking

Speaker: Dr. Cedric F. Lam, Google Inc.
Time: Networking/Light Dinner at 6:00 PM; Presentation at 7:00 PM
Cost: none
Place: Keypoint Credit Union, 2805 Bowers Ave, Santa Clara
RSVP: from the website
Web: ewh.ieee.org/r6/scv/leos

Dr. Cedric F. Lam is currently heading an R&D team working on Google's Fiber-to-the-Home (FTTH) initiative. Prior to starting the FTTH effort, he worked on optical technologies for datacenter networks.

Before joining Google, Cedric was chief system architect at OpVista Inc., responsible for the development of an ultra-dense WDM transport system with integrated ROADM functionality. Prior to OpVista, Cedric was senior technical staff member at AT&T Labs-Research. His research covers broadband optical transport and access networks architectures, optical signal modulation and transmission, passive optical network, HFC, etc. His current focus is in optical networking technologies for data center applications and Fiber-to-the-Home. Dr. Lam received B.Eng. in Electrical and Electronic Engineering from the University of Hong Kong with First Class Honors and PhD. In Electrical Engineering from UCLA.

The author will review the growing trend of warehouse-scale mega-datacenter computing, the Internet transformation driven by mega-datacenter applications, and the opportunities and challenges for fiber optic communication technologies to support the growth of mega-datacenter computing in the next three to four years.

In this talk, we will start from the basic architectural structure of mega data centers, the bandwidth and energy efficiency challenge in scaling datacenter networks. Then we discuss the importance of photonic interconnects in scaling datacenter networks. We will also discuss the myths of photonic switching in data networking applications and compare photonic switching with electronic switching.

OEB Magnetics

WEDNESDAY September 7, 2011

Magnetic Soft X-Ray Microscopy: Imaging Magnetism Down to Fundamental Length and Time Scales

Speaker: Peter Fischer, Staff Scientist, Center for X-ray Optics, Materials Science Division, Lawrence Berkeley National Laboratory
Time: Presentation at 3:00 PM
Cost: none
Place Advanced Light Source, Lawrence Berkeley National Laboratory
RSVP: by email to Dr. Catherine Jenkins, cajenkins@lbl.gov
Web: ewh.ieee.org/r6/oeb/mag

Dr. Peter F ischer received his PhD in Physics (Dr.rer.nat.) from the Technical University in Munich, Germany in 1993 and his habilation from the University in Wuerzburg in 2000 based on his pioneering work on Magnetic Soft X-ray microscopy. Since 2004 he is staff scientist at the Center for X-ray Optics within the Materials Science Division at Lawrence Berkeley National Laboratory in Berkeley. His current research program is focused on the use of polarized synchrotron radiation for the study of fundamental problems in nanomagnetism. He is involved in developing the scientific case for a next generation soft X-ray free electron laser at LBNL. Dr. Fischer has published 125+ peer reviewed papers and has given 135+ invited presentations at national and international conferences. For his achievements of "hitting the 10nm resolution milestone with soft X-ray microscopy" he was co-awarded with the Klaus Halbach Award at the Advanced Light Source in 2010.

One of the scientific and technological challenges in nanomagnetism research is to image magnetism down to fundamental magnetic length and time scales with elemental sensitivity in advanced multicomponent materials. Magnetic soft X-ray microscopy is a unique analytical technique combining X-ray magnetic circular dichroism (X-MCD) as element specific magnetic contrast mechanism with high spatial and temporal resolution. Fresnel zone plates used as X-ray optical elements provide a spatial resolution down to currently 10nm thus approaching fundamental magnetic length scales such as magnetic exchange lengths. Images can be recorded in external magnetic fields giving access to study magnetization reversal phenomena on the nanoscale and its stochastic character with elemental sensitivity. Utilizing the inherent time structure of current synchrotron sources, fast magnetization dynamics such as current induced wall and vortex dynamics in ferromagnetic elements can be performed with a stroboscopic pump-probe scheme with 70ps time resolution, limited by the lengths of the electron bunches.

With a spatial resolution approaching the <10nm regime, soft X-ray microscopy at next generation high brilliant fsec X-ray sources will make snapshot images of nanosclae ultrafast spin dynamics become feasible.

SCV Life Members

MONDAY September 12, 2011

California Water: Crisis or Crossroads?

Speaker: Matthew Heberger, research associate, The Pacific Institute
Time: Dinner at 7:00 PM; Presentation at 7:30 PM
Cost: $15 for dinner (pay at door)
Place: Santa Clara County Office of Education, San Jose Room, 1290 Ridder Park Drive, San Jose
RSVP: By Sept. 3, to Les Besser, LesSCVYes@aol.com (Cancellations by Sept. 10)
Web: not posted

Matthew Heberger is a research associate with the Pacific Institute in Oakland. He has spent the last 15 years working on water issues as a consulting engineer, in water policy in Washington DC, and as a hygiene and sanitation educator in West Africa. He's currently researching issues related to water supply and water quality, water-energy connections, and the impacts of climate change on water resources. Matthew holds a B.S. in Agricultural and Biological Engineering from Cornell University and an M.S.in Water Resources Engineering from Tufts University in Boston and is a licensed professional engineer. The Pacific Institute is a non-profit, nonpartisan research institute that works to advance environmental protection, economic development, and social equity.

Water has become one of California's most polarizing issues, pitting North vs. South, farms vs. cities, and Democrat vs. Republican. Recent news is dominated by stories of drought, shortages, and pollution. Should the state spend billions on new dams and a Peripheral Canal? What can be done to reverse the collapse of once-vibrant salmon fisheries?

Join Pacific Institute research hydrologist Matthew Heberger in a discussion on how insecurity over our most vital resource poses threats to our health, environment, and economy - and how we need to change the way we think about, use, and manage water in the 21st century.

SCV Electromagnetic Compatibility

TUESDAY September 13, 2011

Designing PCB Stackups to Balance Signal Integrity Against Manufacturability

Speaker: Lee W. Ritchey, president, Speeding Edge
Time: Networking and light dinner at 5:30 PM; Presentation at 6:30 PM
Cost: fee for dinner
Place: Applied Materials Bowers Cafeteria, 3090 Bowers Ave., Santa Clara
RSVP: not required
Web: ewh.ieee.org/r6/scv/emc

Founder and president of Speeding Edge, **Lee Ritchey** is considered to be one of the industry's premier authorities on high-speed PCB and system design. He conducts on-site private training courses for high technology companies and also has taught courses for UC Berkeley's extension program as well as industry trade-show technical conferences. In addition, he provides consulting services to top manufacturers of Internet and server products. He is the author of two leading books on high speed design disciplines, "Right The First Time, A Practical Handbook on High Speed PCB and System Design, Volumes 1 & 2". He also the author and publisher of a quarterly newsletter, Current Source, that is dedicated to discussing ongoing topics of concern in the high speed design industry.

Prior to founding Speeding Edge, Ritchey served as Program Manager for 3Com Corporation in Santa Clara, where he was responsible for overseeing the signal integrity aspects of hardware design and product packaging for the company's router, switch, hub and NIC products. Before this, he served as Engineering Manager for Maxtor where he was responsible for the development of high performance disc drives. Previously, he was cofounder and vice president of engineering and marketing of Shared Resources, a design services company specializing in the design of high-end supercomputer, workstations and image products. Earlier in his career, he designed RF and microwave components for the Apollo space program and other space platforms.

Ritchey holds a B.S.E.E. degree from California State University, Sacramento where he graduated as outstanding senior. In 1998, he was profiled by EE Times, as "the high-speed design ratchet man". In 2004, Ritchey began contributing a regular column, "PCB Perspectives" which appears once a month in EE Times.

With the ever increasing speeds of logic and RF systems, the demands placed on PCBs have made it necessary to consider more than impedance when designing the stackup used to for PCB manufacturing. Traditionally, the electronics industry has placed the burden for designing the PCB stackup on the front end engineering personnel at PCB fabricators. While this is convenient for design engineers it places responsibility for several key electrical performance decisions on the fabricator's engineers which they are not equipped to handle. Among those performance decisions are crosstalk rules, impedance targets, interplane capacitance needs and types of weaves that will minimize differential skew between members of a the very high speed differential pairs used in protocols such as PCI Express, XAUI, Double XAUI and other data links that operate at multiple gigabit per second rates.

This session is intended to cover all of the aspects of PCB stackup design from materials choices to arrangement of signal layers and power planes to take the most advantage of the fabrication process. It is taught by an engineer who has been designing PCB stackups for the workstation and super computer marketplace since these products began to be designed and is currently designing stackups for a wide range of products including terabit routers and other products employing signaling protocols to as high as 20 Gb/S. The author has worked with PCB fabricators from the inception of multilayer PCB manufacture and currently works with both fabricators and laminate suppliers to achieve the highest performance from the overall process at the least cost.

SCV Computer, with Signal Processing

TUESDAY September 13, 2011

GPU Computing: Taming a 23,000-Thread Beast!

Speaker: Michael Shebanow, Ph. D., Principal Research Scientist, NVIDIA
Time: Networking with food and beverage at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation helps cover food
Place: Cadence / Bldg 10, 2655 Seely Ave, San Jose
RSVP: from the website
Web: sites.ieee.org/scv-cs

GPUs have fundamentally changed the playing field of high performance computing. Starting out as devices intended only for the display of 3D images, GPUs are now used as supercomputers – attached processors used to accelerate computationally intensive applications. In this talk, using NVIDA GPUs as a basis, I'll provide a brief history of the GPU, the evolution of GPUs into computing devices, understanding their performance characteristics, and the challenges that lie attaining high performance from these devices.

Dr. Michael Shebanow joined NVIDIA in 2003. While at NVIDIA, he has worked on the Tesla product family (G80, GeForce 68xx series) and was one of the lead architects of the Fermi (GF100) family. Also for Fermi, he managed the shader processor architecture team (covered 5 blocks including the SM & L1). He is currently in the research group investigating next-generation graphics and unified programming models for GPUs. Prior to NVIDIA, he has managed the development of a number of processors in multiple architecture families (x86-32, x86-64, SPARC v9, 68k, m88k), and was one of three representatives representing Motorola in the Power PC architecture definition committee. While a graduate student at UC Berkeley, he was one of the original developers of HPS (superscalar, dynamically scheduled processor architectures) (started 1984). Dr. Shebanow holds 25 patents in graphics, processor design, and disk controller areas.

TUESDAY September 13, 2011

Metal Interconnects for Large-area Power Devices: Physics, Challenges, and Solutions

Speaker: Dr. Maxim Ershov, CTO, Silicon Frontline Technologies
Time: Networking and pizza at 6:00 PM; Presentation at 6:15 PM
Cost: none
Place: National Semiconductor, Building E1, Conference Center, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds

Maxim Ershov (Senior member, IEEE) received M.Sc. degree from Moscow Institute of Physics and Technology in 1989, and Ph.D. degree from Russian Academy of Sciences in 1992 in solid state electronics. His research interests are in the areas of semiconductor device physics, numerical simulation, and parasitic extraction. M. Ershov has published over 100 papers in journals and conferences. He has worked at various academic institutions (in Russia, Japan, and the USA) prior to moving to the industrial sector. Ershov's recent experience includes developing innovative semiconductor devices and processes at PDF Solutions, T-RAM Semiconductor, and Foveon. In Silicon Frontline Technology, he is involved in research, development, and applications of mesh-based and meshless field solvers for parasitic capacitance and resistance extraction, simulation, and analysis.

Layouts of multi-layer metallization of large-area power semiconductor devices have a profound effect on device performance and reliability. Metals, vias, and contacts used to route the currents and voltages for source and drain nets impact the metal debiasing, device on-resistance (Rds_{on}), current crowding and current spreading, and uniformity of the current distribution over the area of the device. However, the design, analysis, and optimization of the metal layouts is often driven by rules of thumb, or by the experimental trial and error method, which is very time consuming, costly, and error-prone. Things are further complicated by multiple and frequently changing design rules and constraints related to both on-chip (metal interconnects) and off-chip (leadframe, package, and PCB) requirements. The lack or scarcity of literature on the subject (both textbooks and research publications) makes the problem much worse, especially for non-expert designers and engineers. In this talk, we will review the basic principles of metal layout design for power devices, analyze the underlying physical effects, and highlight typical mistakes. We will also discuss the "best practices" drawn from the analysis, simulation, and optimization of many real design examples. Finally, we will show how using a dedicated simulation software can help to get an insight into the physics of metal interconnects and to guide design optimization.

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WEDNESDAY September 14, 2011

Telemedicine: New Technologies and Perspectives from the Field

Speakers: Dr. Eric Brewer, National Academy of Engineering; Dr. Sudhir (Sid) Ahuja, Vice President, Alcatel-Lucent Ventures; Ravi Amble, serial entrepreneur
Time: Networking, food and drinks at 6:00 PM; Presentations at 6:30 PM, followed by panel
Cost: $5 donation accepted for food & drinks
Place: National Semiconductor Auditorium (Bldg E), 2900 Semiconductor Dr., Santa Clara
RSVP: from the website
Web: www.ewh.ieee.org/r6/scv/comsoc/index.php#sep14

Dr. Eric Brewer focuses on all aspects of Internet-based systems, including technology, strategy, and government. His current focus is (high) technology for developing regions, with projects in India, Ghana, and Uganda spanning communications, health care, education, and e-government. Dr. Brewer co- founded Inktomi Corporation in 1996 and helped create USA.gov working with President Clinton. Dr. Brewer is a member of the National Academy of Engineering. He has received recognition from the World Economic Forum, the Industry Standard, InfoWorld, Technology Review and Forbes.

Dr. Sudhir (Sid) Ahuja leads a team to leverage Bell Labs technology in vertical markets as a Vice President with Alcatel-Lucent Ventures. His current focus is on the Health Care sector. Dr. Ahuja previously served as Vice President of the Convergence, Software, and Computer Science Laboratory at Bell Labs and is a Bell Labs Fellow. Dr. Ahuja is active in IEEE and ACM.

Ravi Amble is a serial entrepreneur actively involved with software-appliance companies that provide solutions for Telemedicine, Continuous Data Protection and Business Continuity, Application-Centric Unified Storage and Enterprise B2B Lead Generation. Ravi previously Co-founded Rapidigm and served as its COO. Rapidigm, an IT Services company, grew to $350 MM in annual revenue in five and a half years and received the recognition as one of Americaâ€™s 500 fastest growing privately held companies for 2 years in a row before being acquired by Fujitsu America in 2006.

Rapid advances in telecommunication technology and growing interest in the efficacy of healthcare have led to mushrooming activity in telemedicine. Recent telemedicine programs are much more ambitious and on a much larger scale than envisioned earlier. We share these with you in this seminar, which includes three talks followed by a panel discussion. Here is a quick overview of each talk:

1. Eric Brewer will describe a novel telemedicine system built by the Technology & Infrastructure for Emerging Regions (TIER) project at UC Berkeley, together with the Aravind Eye Hospital in Tamil Nadu, India. In this solution, rural patients go to local clinics near their village and then meet with (urban) doctors via high-quality videoconference. The TIER program developed and deployed the enabling technology, which is a variation of WiFi that enables high bandwidth over very long distances. The system has been wildly successful with over 300,000 video sessions so far and over 30,000 patients that have had their vision restored. It is also financially self sustaining.

2. Sudhir Ahuja will detail the use of sensor networks and the possibilities they open up for establishing baselines for wellness, detecting early signs of diseases and long term management of diseases. Sensor networking within hospitals enables new capabilities including automatic capture and sharing of clinical data for remote exams and surgery. Such capabilities cause an explosion of event based traffic and require distributed intelligence for data filtering and fusion. The talk will also describe a Telemedicine solution being developed jointly between Alcatel-Lucent and the University of Pittsburgh Medical Center (UPMC) that incorporates these techniques.

3. Ravi Amble, will describe a Telemedicine (Remote Healthcare Monitoring) company called TeleVital, that had its origin in a NASA sponsored research consortium (MedITAC) managed by the Virginia Commonwealth University. TeleVital's product platform, VitalWareâ„¢, is a browser based engine that provides real-time streaming and remote viewing of raw as well as interpreted vital signs and medical images. VitalWareâ„¢ is also integrated with a standards-based, customized multi-media Electronic Medical Record (EMR) system. TeleVital has more than 550 installations in India and has currently established installations in 30 countries out of the 53 African countries under the Pan-African Telemedicine project initiative.

After the presentations, the three speakers will engage in a lively panel session with the moderator and the audience.

WEDNESDAY September 14, 2011

fcCuBE Technology: Expanding the Flip Chip Packaging Landscape

Speaker: Dr. Raj Pendse, VP & Chief Marketing Officer, STATSChipPAC Inc.
Time: Light buffet dinner at 6:00 PM; Presentation (no charge) at 6:45 PM
Cost: $20 if reserved by Sept 12; $10 for fulltime students and currently unemployed; $5 more at door
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: from website
Info: www.cpmt.org/scv/meetings/cpmt1109.html

Dr. Raj Pendse is the Vice President and Chief Marketing Officer at STATS ChipPAC where he is responsible for marketing and business development of the Company's Advanced Technology products. Prior to joining STATS ChipPAC, Raj held various positions in R&D and Package Engineering at National Semiconductor Corp and Hewlett-Packard Labs. His work has spanned the gamut from packaging of high-end microprocessors, ASIC and graphics products to low-cost packaging solutions for logic and analog devices that find use in mobile phones and consumer products. His most recent focus has been on Flip Chip and 3D Wafer Level Packaging. Raj completed his BS in Materials Science from IIT Bombay with Top in Class Honors and his Doctorate in Materials Science from UC Berkeley.

Flip Chip packaging has rapidly evolved into a mainstream solution for a wide range of Computing and Mobile products by virtue of the compelling benefits in performance and small form factors. However, the continued adoption of flip chip technology presents several new challenges. The progressive increase in I/O density with new silicon (Si) nodes creates a widening gap between the escape routing density demanded by the Si device and the design rule roadmap for flip chip substrate technology. Concomitantly, the higher current densities resulting from this I/O density trend bring into play new long term failure mechanisms such as Electromigration. The trend towards Pb-free packaging necessitates bump and interconnect metallurgies that are mechanically damaging to the Si structure further exacerbated by the inherent fragility of the Si by virtue of the use of ELk/ULk (extra or ultra low k) dielectric materials in the newer Si nodes. Last but not the least, the continued deployment of flip chip packaging across a broader range of applications requires that the cost structure be in line with incumbent solutions comprising gold (Au) and copper (Cu) wire bonded packages which use laminate or lead frame substrates.

fcCuBE™ (flip chip with Cu column bump, BOL interconnection and Enhanced assembly processes) technology is a novel solution that systematically addresses the aforementioned challenges. It features the use of Cu column bumps to address the demand of high Si I/O and current densities in conjunction with a proprietary BOL (Bump on Lead) interconnect structure. The unique BOL structure enables remarkable improvement in escape routing density without stretching the substrate design rules while also achieving a dramatic reduction of mechanical stresses in the Si inner layers, thereby essentially eliminating the problem of damage to the Si structure. By virtue of the BOL structure and enhanced assembly processes, notably including Mold Underfilling (MUF), a majority of cost-challenged applications can be packaged in low cost packages with 2-layer laminate substrates comparable in cost to incumbent wire bond solutions.

The key features of fcCuBE technology will be described in detail including the manufacturability and long term reliability of the package. An analysis of the scalability of the approach into the future and the fit of the technology in the overall application space relative to other approaches such as Fan-in and Fan-out Wafer level Packaging.

WEDNESDAY September 14, 2011

Radio-Access LTE-Advanced and Beyond

Speaker: Stefan Parkvall, Ericsson Research, Sweden
Time: Networking, complimentary dinner at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: California Public Utilities Commission, 505 Van Ness Ave (use Golden Gate entrance), San Francisco
RSVP: from the website (for a dinner count)
Web: www.ieee.org/sfcomsoc

Stefan Parkvall is currently a principal researcher at Ericsson Research, working with research on future radio access. He is actively participating in 3GPP physical-layer standardization and is one of the key persons in the development of HSPA, LTE and LTE-Advanced radio access. Dr Parkvall is a senior member of the IEEE and co-author of the popular books "3G Evolution – HSPA and LTE for Mobile Broadband" and "4G – LTE/LTE-Advanced for Mobile Broadband". In 2009, he was co-recipient of the prestigious "Stora Teknikpriset" (Sweden's major technology prize) for his work on HSPA.

He received the Ph.D. degree in electrical engineering from the Royal Institute of Technology in 1996. His previous positions include assistant professor in communication theory at the Royal Institute of Technology, Stockholm, Sweden, and a visiting researcher at University of California, San Diego.

Future Radio Access LTE is rapidly emerging as the dominating 4G standard throughout the world, taking mobile broadband to unprecedented performance levels. The latest version of the LTE standard, known as Rel-10 or LTE-Advanced, by a wide margin fulfills the IMT-Advanced requirements and is one of two technologies approved by ITU as IMT-Advanced compliant. Currently, 3GPP is focusing on Rel-11, taking LTE further beyond the IMT-Advanced requirements.

This talk will provide an overview of the main technology components of LTE-Advanced – enhanced multi-antenna transmission, relaying and carrier aggregation – as well as components such as CoMP and dynamic TDD considered for future LTE releases. In addition to these techniques, meeting future demands for even higher data rates requires a denser infrastructure, for example in the form of a heterogeneous deployment where low-power nodes complement the basic coverage provided by a macro cell.

Such deployments are expected to become increasingly important in the future and may call for enhancements in, for example, inter-cell interference management, as well as further stress the importance of energy efficiency given the large number of nodes. The increasing usage of machine-type communications, where the challenge often is the enormous amount of devices connected rather than the data rates themselves, is another focus area for future radio access. The presentation will discuss these challenges, as well as others, and some technologies for addressing them.

SCV Photovoltaics

WEDNESDAY September 14, 2011

The Consumerization of Energy

Speaker: Craig Lawrence, Ph.D., VP of Products, SunEdison
Time: Networking at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: Palo Alto Research Center (G.E. Pake Auditorium), 3333 Coyote Hill Road, Palo Alto
RSVP: not required
Web: www.svpvs.org

Craig Lawrence is VP of Products at SunEdison, North America's leading solar energy services provider. SunEdison pioneered the Solar-as-a-Service model, and has deployed over 260MW of PV globally and generated over 650 GWh of solar energy since its founding in 2003. At SunEdison, Craig leads new product strategy and product development, with a particular focus on consumer products. Craig also created and led SunEdison's Small Systems business unit, and as General Manager grew SunEdison's presence in the residential and small commercial sectors. Prior to SunEdison, Craig led the Energy Practice at IDEO, a leading design and engineering firm, developing products and services for energy and CleanTech organizations such as the Department of Energy, BP, First Solar, Ford, Rocky Mountain Institute, and Bloom Energy. Craig holds a M.S. and Ph.D. in Mechanical Engineering from Stanford University, and a B.S. from The University of Texas at Austin.

In much of modern society, generations of people have come to accept energy as a given – we flip a switch and we have light. We have become disconnected from the very thing that has enabled our incredible technological and quality of life advancements. But now, we are waking up to the fact that how we get our energy matters – higher energy costs, energy security, dependence on imported fuels, and climate change are poised to fuel a new engagement of consumers with their energy use. This shift creates opportunities for companies to engage consumers and businesses in a new way, and requires energy providers to think beyond the commodity they provide to the experience it creates for customers.

This talk will describe insights gained from the research and development of products for consumers across multiple energy sectors, and discuss how we might apply these lessons to the solar industry.

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OEB Industry Applications

THURSDAY September 15, 2011

Technology Update: Lighting Controls in Commercial and Industrial Applications

Speaker:	Ron France, Leviton Corp
Time:	Social/Networking at 5:30 PM; Presentation at 6:15 PM; Dinner at 7:15 PM; Presentation continues at 8:00 PM
Cost:	$25 for IEEE members, $30 for non-members; $15 for student and retired members
Place:	Marie Zio Fraedos, 611 Gregory Lane, Pleasant Hill
RSVP:	by Sept 12 through Gregg Boltz, gboltz@brwncald.com, Ph: (925) 210-2571
Web:	www.e-grid.net/docs/1109-oeb-ias.pdf

Ron France is a 1985 graduate of Youngstown State University with BSAS degree in Electrical Engineering Technology. He has over 25 years of electrical engineering experience working primarily with URS out of Grand Rapids Michigan. At URS he developed a communications engineering department to design voice, video and data systems and lead the effort to integrate lighting controls and building management systems into the facility design. He has also been a VP of Sales for CTA in Grand Rapids that is a local lighting rep agency in which he was in charge of all technical lines including Levition Lighting Energy Solutions. He has since joined Leviton and relocated to the Bay Area. Ron has always specialized in lighting and lighting control design and is looking forward to conducting a presentation on the latest trends in Lighting Controls, metering, demand response and integration with new lighting technologies. Ron is a local member of IES and the Ben Franklin Club and resides with his family in Antioch.

The discussion will include:

- The current trends in local and national codes affecting lighting controls.
- Centralized and decentralized lighting control systems today and tomorrow.
- Challenges in controlling new lighting technologies.
- Metering and verification with demand response.
- Emergency lighting control options and challenges
- Wireless technologies in lighting control
- Integration with building management systems and challenges.
- The perfect lighting control system!

SCV Nanotechnology

TUESDAY September 20, 2011

Transfer-Printing Semiconductor Nanodevices on Arbitrary Substrates

Speaker: Dr. M. Saif Islam, Department of Electrical & Computer Engineering, UC Davis
Time: Registration & light lunch at 11:30 AM; Presentation at 12:00 Noon
Cost: IEEE Members and Students $5; Non-Members $10
Place: National Semiconductor Bldg E-1 CMA Room, 2900 Semiconductor Drive, Santa Clara
RSVP: from the website
Web: www.ieee.org/nano

M. Saif Islam received his B.Sc. in Physics with Highest Honors from Middle East Technical University; MS degree in physics from Bilkent University (both in Turkey) and Ph.D. degree in electrical engineering from UCLA in 2001. He worked for Hewlett-Packard Laboratories and SDL Inc./JDS Uniphase Corporation before joining UC Davis in 2004, where he is a Professor now. His work covers ultra-fast optoelectronic devices, molecular electronics, and integration of semiconductor nanostructures in devices for imaging, sensing, computing and energy conversion. He has authored/co-authored more than 160 scientific papers, edited 15 books and conference proceedings and holds 36 patents as an inventor/coinventor. Dr. Islam received NSF Faculty Early Career Award, Outstanding Junior Faculty Award, IEEE Best Paper Award,

An experimental method will be presented for fabricating large area, high performance single crystal devices via both top-down and bottom-up techniques and transferring them to low cost carrier substrates while simultaneously preserving the integrity, order, shape and fidelity of the transferred device arrays. The original substrates are repeatedly used for continual production of new devices and are minimally consumed. This greatly decreases the cost of device fabrication by dramatically reducing the material consumption and making it an environmentally benign process while offering high performance, flexibility, ease of packaging and integration. This heterogeneous integration technique offers the ability to integrate various single crystal nanodevices on a variety of substrates for large-scale applications in energy conversion, sensing, computing and micro/nanophotonics.

SCV Consultants' Network of Silicon Valley

TUESDAY September 20, 2011

IP Strategies for the New Decade

Speaker: Charles W. McLaughlin, Fergason Licensing, LLC
Time: Presentation at 7:00 PM
Cost: none
Place: KeyPoint Credit Union, 2805 Bowers Ave., Santa Clara
RSVP: not required
Web: www.CaliforniaConsultants.org

Chuck McLaughlin is a founder of and Managing Partner at Fergason Licensing in Menlo Park, where he has served as the licensing agent for Fergason Patent Properties (FPP). Working closely with inventor Jim Fergason, Chuck developed a positioning strategy for FPP's dynamic contrast technology. He launched a licensing program that has resulted in licenses with more than 25 major LCD display companies including Panasonic, LGD, Sharp, Samsung and AUO.

Chuck holds a BS in Chemical Engineering from Drexel University and an SM in Industrial Management from MIT's Sloan School.

As the electronics market and technology matures, the role of intellectual property (IP) is evolving. Using a successful LCD technology and IP licensing program that he established as an example, Chuck McLaughlin will share his views regarding viable IP strategies for the coming decade.

Chuck's presentation will include the following topics:

Recent trends in electronics IP
Major IP players and their strategies
IP monetization paths and expectations
Directions for independent inventors and startups

Since the creation of IP is often a critical aspect of a consulting engagement, it is important to understand how to leverage your expertise in this context.

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SCV Power Electronics

WEDNESDAY September 21, 2011

Better Place – The Storage Story for Vehicles

Speaker: Hugh McDermott, Vice President Global Utilities & Energy, Better Place
Time: Networking & Pizza at 6:00 PM; Presentation at 6:30 PM
Cost: none
Place: National Semiconductor, Building E Auditorium, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/pels

Mr. Hugh McDermott is the Vice President Global Utilities & Energy where he leads Better Place utility partnering and energy services initiatives.

Mr. McDermott possesses over 25 years of experience in energy technology and energy infrastructure development encompassing over 40 countries. His career background includes executive management, business development, and project management roles involving development of large energy infrastructure projects and clean technologies. Prior to joining Better Place, Mr. McDermott served as senior vice president of Nexant, where he was a founding management team member and lead the firm's emerging markets and utility practices. Mr. McDermott is a frequent speaker in clean-tech and utility industry forums around the world and has served on numerous advisory panels including a recently appointment by US Secretary of Commerce to serve on the U.S. Industry Trade Advisory Committee on Energy in support of international trade development for the US energy industry. Mr. McDermott holds a B.S. in mechanical engineering in power systems from Virginia Tech.

Better Place is a global electric vehicle network operator and most known for the concept of battery switching to enable range extension and a "no-compromise" solution for drivers to make the switch to electric vehicles. What is less known publicly is the ability of BP to operate its networked charging infrastructure as a virtual generator and electric grid storage asset in coordinate with utility and grid operations. With little or no operating cost, utility integrated EV charging operations could be the "killer app" for utility-scale storage. This talk introduces Better Place from a utility operations perspective and will share how networked and centrally controlled EV charging infrastructure could become the "smartest part of the smart grid" for a generation to come.

WEDNESDAY September 21, 2011

Electric Vehicle (EV) Technology & Tour of KLEENSPEED Technologies

Speaker: Dante Zeviar, Executive Vice President and Chief technology Officer, KleenSpeed
Time: Networking & pizza at 6:00 PM; Presentation/Tour at 7:00 PM
Cost: none
Place: KLEENSPEED Technologies, Inc., Moffett Research Park, Building 554 on Cody St., Moffett Field
RSVP: by email to Fred Jones, frederick.m.jones@nasa.gov, (650) 604-2521
Web: www.e-grid.net/docs/1109-scv-pes.pdf

Dante Zeviar, Executive Vice President and Chief technology Officer: B.Sc. in Mechanical Engineering from University of California at Berkley, M.Sc. in Automotive Engineering from Technical University of Munich in Germany, Professional Automotive Technician from Universal Technical Institute, developed formula-style race cars, worked in R&D at BMW and developed an aluminum electrical connector for high current application in hybrid and electric vehicles.

KLEENSPEED is an R&D Company focused on the development of innovative and advanced technologies and intellectual properties that will revolutionize the EV industry and create systems and vehicles that truly realize the full potential of electric vehicles.

The company's agenda is clearly drawn to tackle and resolve the challenging issues regarding the development of breakthrough solutions to EV systems design and development.

KLEENSPEED is passionate about EV technology as a viable solution to many environmental issues. We believe that the wide spread adoption of electric vehicles will lead to a better way of life. They are convinced of the near-term potential and the long-term future of electric vehicles from a business perspective. We are committed to being a leader in EV technology and business.

The Electric Vehicle has been in existence since the dawn of the automotive age at the turn of the 20th century. Yet, despite the considerable potential and environmental advantages of this technology, all EVs to date have had limited functionality and viability in the consumer marketplace.

KLEENSPEED is focused on the development of innovative and advanced technologies that will revolutionize the industry and create systems and vehicles that truly realize the full potential of electric vehicles. Founded by Tim Collins, a technology visionary with a career of success in technology businesses and investment banking, and driven by an R&D team led by Dante Zeviar, a brilliant young engineer, KLEENSPEED is already a proven leader in EV technology.

The company's agenda is clearly drawn to tackle and resolve the challenging issues regarding the development of breakthrough solutions to EV systems design and development.

Their EV-X11 race car and the EIATA sports car will be at the site.

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THURSDAY September 22, 2011

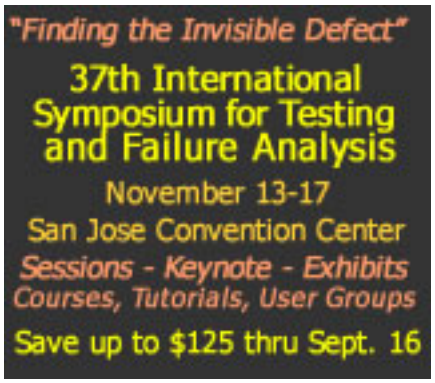
Memory Scaling and Its Potential Impact on Computing and Storage

Speaker: Ed Doller, VP and Chief Memory Systems Architect, Micron Technology
Time: Registration at 11:30 AM; Buffet lunch at 11:45 AM; Presentation at 12:15 PM
Cost: $15 if reserved by Sept 20; $5 for fulltime students and currently unemployed; $5 more at door
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: from website
Info: www.cpmt.org/scv/meetings/cpmt1109l.html

As memory technologies scale current memory, usage models will be challenged. While new emerging technologies hold promise to solve the scalability challenge, it is unlikely that they will be "drop in compatible" with current technologies and thus will impact current memory hierarchies and utilization in the compute and storage segments. At the same time, lines are beginning to blur both in the compute segment and the storage segment as the debate over direct-attached storage is heating up –- again. Ed Doller, VP of Micron's architecture research and development team, will explore the impact of scalability on current memory technologies, discuss what technologies may be next, and assess the impact of both of these on computer and storage architectures and on packaging options.

Ed Doller is Vice President and Chief Memory Systems Architect at Micron Technology. Mr. Doller joined Micron in May 2010 from Numonyx where he served as Chief Technology Officer after its formation in 2008. Before Numonyx, Mr. Doller had a variety of roles in the Flash memory group at Intel, and then was appointed its Chief Technology Officer in 2004. Prior to Intel, he held several key positions at IBM in East Fishkill, N.Y., all in advanced semiconductor memories.

Mr. Doller earned a Bachelor of Science degree in computer engineering from Purdue University. He has more than 27 years of experience in semiconductor memories, holds multiple patents, is a co-author of the IEEE floating gate standard, and is a frequent keynote speaker at memory conferences.



SCV Circuits and Systems

MONDAY September 26, 2011

Video Compression Technology – Building the Next Generation

Speaker: Prof. Nam Ling, Santa Clara University
Time: Networking, light dinner at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation accepted for food
Place: QualComm, Building B, 3165 Kifer Road, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/cas

Nam Ling received B.Eng. from Singapore, and M.S. and Ph.D. degrees from U.S.A. Since 2010, he is the Sanfilippo Family Chair Professor of Santa Clara University and the Chair of its Department of Computer Engineering. He was an Associate Dean (Graduate Studies, Research, and Faculty Development) for its School of Engineering during 2002-2010. Currently he is also Consulting Professor for the National University of Singapore and Guest Professor for Shanghai Jiao Tong University. Dr. Ling is an IEEE Fellow for contributions to video coding algorithms and architectures. He is also an IET Fellow. He has more than 150 publications and standards contributions, including a book. He was named IEEE Distinguished Lecturer twice and received the IEEE ICCE Best Paper Award (First Place). He received four major awards from the University (Outstanding Achievement, Recent Achievement in Scholarship, President's Recognition, and Sustained Excellence in Scholarship) and two awards from its Engineering School (Researcher of the Year and Teaching Excellence). He served as Keynote Speaker (IEEE APCCAS, VCVP, JCPC, and will be for the coming IEEE ICAST and ICIEA), Distinguished Speaker (IEEE ICIEA), General Chair/Co Chair (IEEE Hot Chips, VCVP), Technical Program Co Chair (IEEE ISCAS, APSIPA ASC, IEEE APCCAS, IEEE SiPS, DCV), and Technical Committee Chair (IEEE CASCOM TC and TCMM). He also served as Guest Editor/Associate Editor for journals (IEEE TCAS I, JSPS) and delivered more than 110 invited colloquia worldwide.

In recent years, a significant increase in visual resolution and perceptual quality has emerged. Another level of resolution and quality will be expected for home and mobile video applications as future devices and content move toward high definition (for mobile applications) and ultra-high definition (for home applications). Existing AVC/H.264 video compression technology will soon be unable to efficiently meet the compression demands for transmission. With the recent work from the Joint Collaborative Team on Video Coding (JCT VC) High Efficiency Video Coding (HEVC) project, a new generation of video compression standardization process aiming at major improvements over the current AVC/H.264 standard has already begun. In this talk, we will briefly look at the expectation and the building of the technology for next generation video compression; we will also highlight our experience and work in this area.

SCV Information Theory

WEDNESDAY September 28, 2011

The Role of Information Theory in Public Key Cryptography

Speaker: Dr. Martin E. Hellman, Professor Emeritus of Electrical Engineering, Stanford University
Time: Refreshments at 5:30 PM; Presentation at 6:00 PM
Cost: none
Place: 202 Packard Bldg, Stanford University, Stanford
RSVP: not required
Info: Art Astrin, art_astrin@yahoo.com

Prof. Martin E. Hellman received his B.E. from New York University in 1966, and his M.S. and Ph.D. from Stanford University in 1967 and 1969, all in Electrical Engineering.

Prof. Hellman was at IBM's Watson Research Center from 1968-69 and an Assistant Professor of EE at MIT from 1969-71. Returning to Stanford in 1971, he served on the regular faculty until becoming Professor Emeritus in 1996. He has authored over seventy technical papers, six US patents and a number of foreign equivalents.

Hellman is best known for his invention, with Diffie and Merkle, of public key cryptography. In addition to many other uses, this technology forms the basis for secure transactions on the Internet. He has also been a long-time contributor to the computer privacy debate, starting with the issue of DES key size in 1975 and culminating with service (1994-96) on the National Research Council's Committee to Study National Cryptographic Policy, whose main recommendations have since been implemented.

People are often surprised that public key cryptography was invented within Stanford's EE department, not the Computer Science department. Yet my background in Information Theory played a key role in that advance. This talk reviews my professional odyssey, from research in more traditional information theory to cryptography to estimating the odds that civilization will survive another century. The unifying theme is the role that my training in information theory played in guiding that journey.

SCV Photonics

TUESDAY October 4, 2011

Green Photonics Trends for the Next Decade: Communications, Lighting, Solar

Speaker: Michael Lebby, GM and CTO, Translucent Inc.
Time: Networking/Light Dinner at 6:00 PM; Presentation at 7:00 PM
Cost: none
Place: Keypoint Credit Union, 2805 Bowers Ave, Santa Clara
RSVP: from the website
Web: ewh.ieee.org/r6/scv/leos

In April 2010, **Michael Lebby** joined Translucent Inc. based in Palo Alto, to head up the company's R&D efforts to commercialize rare earth oxides for epitaxial-based materials that have been developed over the past decade. Crystalline-based semiconductor rare-earth oxides exhibit a number of attractive properties for advanced substrate and device solutions that include GaN-on-Si for solid state lighting and power electronics, Ge-on-Si for CPV solar and GaAs based photonics and electronics.

Lebby led the drive for green photonics while heading OIDA in the mid 2000s. The adoption and acceleration of this new discipline has become a significant focus for the photonics industry.

Lebby's career has spanned all aspects of the optoelectronics business ranging from research and development, operations, manufacturing, and finance, to sales, marketing, and investing. Lebby has worked at RSRE for the British Government in the UK, AT&T Bell Labs, Motorola, Tyco Electronics, Intel, Ignis Optics (VC backed start-up that was sold to Bookham - now Oclaro), OIDA, and presently, Translucent.

With more than 180 USPTO utility patents issued in the field of optoelectronics, Lebby has been cited by the USPTO to be in the most prolific 75 inventors in the country from 1988-1997. Lebby is a Fellow member of IEEE and OSA, and has testified on behalf of the optoelectronics industry while working for OIDA on Capitol Hill. Lebby has given numerous talks, speeches, panel discussions, and interviews, on the subject of optoelectronics internationally over the past two decades. Lebby has 2 doctorates and a MBA from the University of Bradford in the UK.

Photonics technologies and products that have been based on semiconductors have experienced significant growth over the past decade, with examples from many consumer and fiber communication products that contain; lasers, displays, solar cells, and LEDs. This talk will review the status of green photonics as it relates to the photonics field, and will explore how the technologies will develop into more exciting products over the next decade.

One example of a new green photonics opportunity is figuring how to put photonics technologies onto large silicon wafers. The talk will show that compliant, lattice matched rare earth oxides (REO) for GaN-on-Si and Ge-on-Si offer a scalable solution that is cost effective and exciting.

- Ge-on-Si using REO will enable large, low cost semiconductor platforms for multi-junction high efficiency photovoltaic, solar cells, GaAs based photonics for communications, and GaAs electronics on silicon wafers.
- GaN-on-Si using REO will enable large, low cost semiconductor platforms for energy efficient Power FETs and high performance LEDs for solid state lighting

Green photonics technology and market philosophy has been evolving for years as a large portfolio of engineers and scientists strive for energy efficiency, cleaner solutions and improved health in their designs. Traditional photonics segments such as fiber communications, photonic lighting, solar, optical networking, and photonic device integration make up some of the green photonics segment. Data presented from OIDA based in Washington DC., will show that many classic photonic fields will become more 'green' through more efficient product design over the decade.

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SCV Technology Management

THURSDAY October 6, 2011

Product Management for Project and Program Managers

Speaker:	Rich Mironov, serial entrepreneur and author
Time:	Networking at 6:00 PM; Forum at 6:30 PM; Dinner at 7:15 PM; Presentation at 7:45 PM
Cost:	$10 for IEEE members; $13 for others (through Oct 4)
Place:	RAMADA Silicon Valley, 1217 Wildwood Ave, Sunnyvale
RSVP:	not required
Web:	www.ieee-scv-tmc.org

Rich Mironov is a serial entrepreneur, and currently CEO of a stealth startup. At earlier companies and consulting stints, he's been VP Product Management/ VP Marketing, the go-to-market strategist and agile "product guy". Rich is a veteran of four previous tech start-ups and dozens of consulting engagements. From 2006 through 2010, he provided full-time and interim consulting/mentoring to large and small technology companies.

Rich's 2008 book, "The Art of Product Management," captures the best of Product Bytes from 2001 to 2008, and represents the scrappy entrepreneur in all of us. Rich serves on the board of SVPMA, has taught in Haas' executive education program, and produced (chaired) the product manager/product owner track for Agile Alliance's 2009 and 2010 conferences. He is an in-demand speaker for business, executive and technical audiences.

Since 2001, Rich has been an interim executive, consultant or adviser to dozens of early-stage companies and larger technology firms including Yahoo, Cisco, Varian and VeriSign. From 2007 to 2009, he was CMO of Enthiosys, an agile product management consultancy.

Rich and Enthiosys also founded the first P-Camp, now spreading around the country as Product Camps. These semi-unstructured get-togethers provide product managers an opportunity to network, teach, learn and share.

Rich has a BS in Physics from Yale with a thesis on dinosaur extinction theories, and an MBA from Stanford.

This will be a VERY spirited discussion…

We will gather some (good and bad) experiences from attendees about their interactions with product management, try to define what the PM role is, and share some thoughts on how to cooperate better for great products and organizations. Lots of questions about how to get into product management, and why people would stay in such a role!

Our focus will be on first-line and second-line development managers, whose teams interact directly with product managers, and those that work with these teams.

WEDNESDAY October 12, 2011

Silicon Carbide (SiC) Sensing Technology for Extreme Harsh Environments

Speaker: Debbie G. Senesky, Ph.D., University of California, Berkeley
Time: Optional buffet dinner at 6:00 PM; Presentation (no charge) at 6:45 PM
Cost: $20 per person; $10 for fulltime students and currently unemployed engineers; $5 more at the door
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: From website
Info: www.cpmt.org/scv/meetings/cpmt1110.html

Debbie G. Senesky received the B.S. degree in mechanical engineering from the University of Southern California, Los Angeles, in 2001, and the M.S. and Ph.D. degrees in mechanical engineering from the University of California, Berkeley, in 2004 and 2007, respectively. From 2007 to 2008, she was a Microelectromechanical Systems Design Engineer for GE Sensing (formerly known as NovaSensor). She is currently a Research Specialist at the Berkeley Sensor and Actuator Center, UC-Berkeley. Her research interests include the development of silicon carbide (SiC) micro- and nano-systems, harsh environment materials, sensor technology and energy conversion.

This presentation discusses advances in SiC manufacturing technology including growth of amorphous SiC thin films, polycrystalline SiC thin films and high-temperature metallization. Results of fabricating micro-scale SiC sensors and operating SiC sensors within high temperature (600oC), dry steam and high shock environments are presented. The stability of high-temperature metallization and ceramic packaging for SiC components will also be discussed.

Harsh environment sensors can be used to perform real-time, in-situ combustion monitoring leading to designs of power and propulsion systems (e.g. industrial gas turbines, and aircraft engines) with increased efficiencies, fuel flexibility and reduced CO2 emissions. Space exploration can be extended with high temperature, radiation-hardened materials, instrumentation and energy conversion devices using Silicon carbide (SiC), a ceramic, semiconductor material that is stable in high temperature, high radiation and chemically corrosive environments.

SCV Consultants' Network of Silicon Valley

TUESDAY October 18, 2011

Leveraging Consulting to Build a Bionic Technology Company

Speaker: Robert Horst, Ph.D., Tibion Corp.
Time: Presentation at 7:00 PM
Cost: none
Place: KeyPoint Credit Union, 2805 Bowers Ave., Santa Clara
RSVP: not required
Info: www.CaliforniaConsultants.org

Robert Horst is the founder and VP of R&D at Tibion Corp. He has over ten years of experience designing products for robotic therapy and mobility enhancement. Bob has over 30 years of experience in electronics, systems architecture and fault-tolerant computing from his tenure at Hewlett Packard, Tandem Computers, Compaq, 3ware, and Network Appliance.

As a consultant, he has worked with several startup companies and served as an expert witness in patent litigation. Dr. Horst is an IEEE Fellow and currently holds 73 US patents. He received a BSEE from Bradley University, an MSEE from the Univ. of Illinois and a Ph.D in Computer Science from the Univ. of Illinois.

Consulting can play a key role in supporting entrepreneurs while they develop new technologies to the point where the ideas are mature enough to attract outside investors. The right mix of consulting and startup work can provide the freedom to pursue unconventional products, technologies and markets.

This talk will focus on the pursuit of wearable, assistive, mobility devices at Tibion Corp. Consulting income was a key to Tibion's survival from initial ideas in 2001 to first venture funding in 2006 and on to product introduction in 2010. Topics to be discussed include:

- iterating to find and perfect the right technologies
- building prototypes for early market feedback
- addressing medical device challenges: reimbursement, quality systems and FDA clearances
- building a business that meets VC investment objectives
- market focus and clinical validation
- lessons learned

The first Tibion product - the Bionic Leg - is now in use at several clinics across the country. The operation of the Bionic Leg will be illustrated by videos of patients undergoing therapy to address neuromuscular deficiencies.

FRIDAY October 21, 2011

Quality: On the Road to Performance Excellence

Speakers: over 20 talks in 5 tracks
Time: Registration at 7:30 AM; Seminar from 8:30 AM - 5:00 PM; Reception/talk in evening
Cost: $120 members, $145 non-members (thru Aug 31); afterwards: $150/$180
Place: Techmart, 5201 Great America Parkway, Santa Clara
RSVP: from website
Info: www.asq-silicon-valley.org/quality-conference

Schedule

7:30-8:30 Registration, Raffle Tickets, Continental Breakfast (Coffee, Tea, Bagels, etc.)

8:30-8:35 Opening Welcome: Conference Co-chair Ms. Christina DeLeon

8:50-9:45 Break-out Session 1

10:00-11:00 Morning Keynote:
Achieving Performance Excellence in Every Product and Process
Introduction by Section Chair Doug Chapman;
Keynote Speaker: Dr. Thomas A. Little, President Thomas A. Little Consulting

11:10-12:00 Break-out Session 2

12:00-1:30 Lunch Buffet
12:15-12:45 (Optional) Employment Session: Ms. Joan Cheng
12:15-12:45 (Learning Lunch) Project Selection; Picking Winners: Mr. Ed Russell

1:30-2:30 Break-out Session 3

2:40-3:40 Break-out Session 4

4:00-5:00 Afternoon Keynote
The Five Pillars of Organizational Excellence
Introduction by Program Chair Dr. John J. Flaig
Keynote speaker: Dr. H. James Harrington, CEO The Harrington Institute
Keynote speaker: Mr. Chuck Mignosa, Owner, President & Principal Consultant at Business Systems Architects LLC

5:00-5:05 Announce collection of conference evaluations at 5:30 (Mr. Sid Dutta)
5:05-5:30 Recognize Volunteers & Sponsors: Conference Co-chair Mr. Sid Dutta
5:30-5:40 Collect Conference Evaluation forms and distribute Raffle tickets
5:40-5:50 Raffle

5:50-6:30 Presentation “Making Quality Magical” by Mr. Chuck Mignosa
6:30-7:30 Networking Mixer (music, snacks, open bar, one drink on US)

See website to download details for presentations.