CHAPTER MEETINGS

SCV-VT - 8/29 | **Automated Transit Networks** - driverless vehicles, fixed trackways, high traffic densities, control technology ... [more]

SCV-TMC - 9/6 | **Management Myths and Time Span Inconsistencies** - scientific findings, complexity, hiring process, level of work ... [more]

SCV-GOLD - 9/8 | **Woodside Hike, Huddart County Park** - 4.5 mile loop, 2 1/2 hours, social time with other members ... [more]

SCV-SECTION+PACE - 9/10 | **IEEE Senior Member Grade Elevation Night** - what it takes to be Sr Member; details; drop-in ... [more]

SCV-Life - 9/10 | **Virtual Worlds: Technology, Imagination and the Future of Play** - immersive, physics-based, avatars, richness ... [more]

SCV-CS - 9/10 | **Silicon Convergence: Creating System Solutions with Coarse- and Fine-grained Programmable Hardware** ... [more]

SCV-EMC - 9/11 | **Smart Grids, Worse Power Quality, and Conducted 2kHz-150kHz EMC: Practical Experience Around the World** [more]

SCV-CPMT - 9/12 | **Additive Manufacturing -- It's Not Always Rapid And It's Not Just For Prototypes** - real-time, volume, examples . [more]

SCV-CAS+SSC - 9/12 | **2D to 3D MOS Technology Evolution for Circuit Designers** - fundamentals, mechanical strain, high-k, ... [more]

SCV-PACE - 9/12 | **Career Networking Night** - job-seekers, meet employers, hiring-focused ... [more]

SCV-Mag - 9/18 | **Microwave-Assisted Magnetic Recording** - superparamagnetic limit, new approaches, rf fields, results ... [more]

OEB-NPSS - 9/18 | **Discovery/Development of Improved Scintillation Detector Materials for Medical Imaging and National Security** [more]

SCV-CNSV - 9/18 | **Beyond Virtualization: A Novel Software Architecture for Complex Multi-Core SoCs** - multiple cores, OS, limits . [more]

SCV-Nano - 9/18 | **Nanotechnology-Enabled Redox-Flow Batteries Give the Smart Grid a High IQ** - safe, reliable, distributed ... [more]

OEB-PES - 9/19 | **Underwriters Laboratories (UL) Tour** - products tested, high-tech, power, controls, appliances, certifications ... [more]

OEB-IAS - 9/20 | **Combining Power System SCADA and PMCS Software into One Solution: A Hybrid Approach** - applications [more]

SCV-GOLD - 9/22 | **High-Impact Interpersonal Communications: How to Communicate with Anyone, Anywhere** – seminar ... [more]

SCV-CPMT - 9/27 | **The Origins of Silicon Valley: Why and How It Happened Here** - 1910-1950's, radio tubes, Stanford, processes . [more]

SCV-ComSoc+CAS - 9/29 | **Next Generation Circuits & Systems, Communications and Sensor Technologies in Mobile Devices** [more]

SCV-EMC - 10/11 | **ESD Troubleshooting Techniques for Electronic Designs; Fundamentals of Signal and Power Integrity** – symp. [more]

SCV+OEB-Life - 10/13 | **Motivating Our Students to Become Engineers: How You Can Make It Happen** - half-day forum ... [more]

Conference Calendar

Sept 11-13: **Complex Aerospace Systems Exchange** - Pasadena Convention Center [more]

September 28-29: **IEEE Career Strategy and Smart Tech Professional Workshop** - Santa Clara Conv'n Ctr [more]

Oct 7-10: **Int'l Conference on Very Large Scale Integration (VLSI-SoC)** - Dream Inn, Santa Cruz [more]

Oct 21-24: **Global Humanitarian Technology Conference** - Renaissance Seattle Hotel [more]

Nov 4-7 : **45th Annual Asilomar Conf on Signals, Systems, and Computers** - Pacific Grove [more]

Nov 11-15**: 38th Int'l Symposium for Testing and Failure Analysis** - Phoenix Convention Center [more]

Dec 3-7: **IEEE Global Communications Conference (GlobeCom)** - Disneyland Hotel, Anaheim [more]

Calls for Papers:

Int'l Symposium on Quality Electronic Design (ISQED)

Interdisciplinary Engng Design Education Conference

- March 4-6, 2013 - TechMart, Santa Clara [more]
- Papers due **September 12**

Santa Clara University Grad School of Engineering

Fall Open University [more]

- Early-morning, evening, Saturday classes

IEEE Chapter Seminars, Workshops

Sept. 22: **High-Impact Interpersonal Communications: How to Communicate with Anyone, Anywhere -- Get More Results with Everyone, Everywhere** - trust, rapport [more]

Sept. 29: **Next Generation Circuit & Systems, Communication and Sensor Technologies in Mobile Devices** One-day Weekend Workshop -- Santa Clara [more]

Oct 11: **ESD Troubleshooting Techniques for Electronic Designs; Fundamentals of Signal and Power Integrity-** One-day Weekend Workshop -- Santa Clara [more]

Career Development

Professional Skills Courses [more]

- Consulting Skills for Engineers - 5 Habits of Intentional Leadership - Communicating Across Cultures - Project Management: A Team Approach - Emotional Intelligence *… and more*

Support our advertisers

MARKETPLACE – Services **page 3**

IEEE GRID

Your Networking Partner®

September 2012 • *Volume 59 • Number 9*

IEEE-SFBAC
PO Box 2110
Cupertino, CA 95015-2110

IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for news for technologists, managers and professors, the editorial objectives of IEEE **GRID** are to inform readers of newsworthy IEEE activities sponsored by local IEEE units (Chapters, Affinity Groups) taking place in and around the Bay Area; to publicize locally sponsored conferences and seminars; to publish paid advertising for conferences, workshops, symposia and classes coming to the Bay Area; and advertise services provided by local firms and entrepreneurs.

IEEE GRID is published as the **GRID** Online Edition residing at www.e-GRID.net, in a handy printable **GRID.pdf** edition at the end of each month, and also as the **e-GRID** sent by email twice each month to more than 24,000 Bay Area members and other professionals.

Editor: Paul Wesling
IEEE **GRID**
PO Box 2110
Cupertino CA 95015-2110
Tel: 408 331-0114 / 510 500-0106 /
415 367-7323

Fax: 408 904-6997
Email: editor@e-grid.net
www.e-GRID.net

From the Editor

MONEY Magazine often has helpful articles about managing resources, planning your financial future, and other topics. Last month we covered this one:

Don't wait for your company to train you.

I'd like to focus now on the second piece of their advice:

Be an expert, not an employee

"Write papers, give speeches, get involved in leadership positions with professional organizations and associations within your field. It'll reaise your profile and expand your network."

Is this something you now focus on consciously? It can be intimidating to begin asserting yourself as an expert in your chosen field, or in an emerging one. That's where the IEEE comes in – with volunteer leadership opportunities, conferences where you can give papers and meet peers, and many networking opportunities.

If you continue to concentrate on just "doing your job" but neglect these "outside activities," you'll find others getting the preferred positions, helping make the decisions, and falling farther behind. So, look for the next Call for Papers from a conference in your field, and talk to the officers of your local IEEE chapter to see if you can help them organize programs. Look for chances to make an impact in your company.

Keep your career moving upward – use your local IEEE's resources to get ahead!

Best regards,

Paul

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

Professional Services Marketplace – editor@e-GRID.net for information

Say you found them in our GRID MARKETPLACE

Santa Clara University School of Engineering Graduate Programs

SCU Fall Open University

Have you ever wanted to continue your education in engineering while you continued working? Santa Clara University's School of Engineering offers graduate degree and non-degree programs to both full-time students and working professionals. Simplified registration for the Spring Open University. Graduate-level instruction. Up to 16 units may be transferred to a graduate-degree program.

Early-morning classes:
- Linear Algebra - Speech Coding - Applied Math - Intro to Systems Engineering *(and more)*

Evening classes:
- Web Architecture & Protocols - Logic Design Using HDL - IC Fab Processes - Nanoelectronics *(and more)*

Saturday classes:
- Wireless Mobile Networks - Design of SOCs - Law, Technology, IP *(and more)*

Email LeAnn Marchewka with inquiries:
LMarchewka@scu.edu

Santa Clara University

Prepare for that next project or assignment!

To remain competitive in Silicon Valley's changing environment, engineers need to update their knowledge base. The School of Engineering offers professional Certificates and Open University programs, as well as graduate degrees, for those who are driven to become leaders in their fields.

- **Registration now open**
- **Classes begin September 19**

Located in the heart of Silicon Valley, with easy parking

Review autumn Open University courses:

www.scu.edu/engineering/graduate

GLOBAL HUMANITARIAN TECHNOLOGY CONFERENCE

October 21-24, 2012
Renaissance Seattle Hotel
Seattle, Washington

IEEE has a strong focus on applying technology for the benefit of humanity. GHTC has these goals:

- Foster exchange of information and networking in the humanitarian field
- Focus attention of businesses on emerging market opportunities and related technology enablers
- Impact in positive and meaningful ways the lives of disadvantaged billions of people around the world
- Promote science, engineering and technology as key to development of solutions for disadvantaged communities and attract young people to these professional fields

Keynote speakers

● Krista Bauer, GE Foundation ● Gordon Day, IEEE President and CEO ● Jim Fruchterman, Benetech ● Robert A. Freling, Solar Electric Light Fund (SELF) ●Gretchen Kalonji, UNESCO ● Peter Staecker, IEEE President-Elect ● Gertjan van Stam, IEEE HTAC ● Byron Reese, Demand Media ● Knut Aanstad, Advisor, UN Sustainable Energy for All

GHTC 2012 Topics:

- Health, Medical Technology, Telemedicine
- Disaster Warning, Avoidance, and Response
- Water Planning, Availability and Quality, Sanitation
- Power Infrastructure/Off-grid Power/Renewable and Sustainable Energy
- Connectivity and Communications Technologies (data/voice) for Remote Locations
- Educational Technologies
- Agricultural Technologies
- Applying Science, Engineering and Technology for Environmental Sustainability

Panel Sessions

● Transitioning from the For-profit to the Non-profit World ● Improving Access to Quality Care: Rising to the Challenge in Resource-Poor Settings

Register today – save, through September 7th!

www.ieeeghtc.org

International Conference on Very Large Scale Integration (VLSI-SoC)

October 7-10, 2012
Ocean-Front: Dream Inn, Santa Cruz

Come explore the state-of-the-art and new developments in Very Large Scale Integration (VLSI), System-on-Chip (SoC) and their designs – a forum to exchange ideas and show industrial and research results in the fields of VLSI/ULSI Systems, SoC design, VLSI CAD and Microelectronic Design and Test.

Topics include: ● Analog and Mixed-Signal IC design ● Microsystems and integrated MEMS for bio-systems ● Design for variability, reliability, fault tolerance, test ● Circuits and systems for DSP, image processing, communications ● Emerging technologies and new devices ● Prototyping, verification, silicon debug for SoCs ● 2D- and 3D-interconnect architectures, topologies ● System-on-chip, embedded VLSI systems, multi-core systems ● Reconfigurable systems, application-specific processors, FPGAs ● Digital VLSI circuits, memories ● Logic and high-level synthesis, SW synthesis, HW-SW co-design ● Low-Power and Temperature-Aware design

Save $200 -- Early registration ends August 31!

More infromation at

vlsisoc2012.soe.ucsc.edu

Special Sessions

Memristive Computing

Memristors and memristive devices have recently been realized at nanoscale. Several recent implementations have brought forth the potential for revolutions in non-volatile storage and reconfigurable computing. This special session is specifically focused at using memristive devices for computing in programmable systems such as FPGAs.

Open Source Tools and Methodologies for Research

Open source tools enable both academia and industry to research, develop, and share common platforms in complex research tasks. However, most often these open source tools and methodologies are unsung and, in fact, difficult to publish. This special session is specifically focused on recognizing the most important and useful open source tools and methodologies that aid research.

Asilomar Conference on Signals, Systems, and Computers

ASILOMAR CONFERENCE GROUNDS
PACIFIC GROVE
November 4-7, 2012

The **Asilomar Conference on Signals, Systems, and Computers** is a forum for presenting work in various areas of theoretical and applied signal processing.

75 Sessions, including: ● Graphical Models in Signal Processing ● Green Radio ● Voice Coding ● Full-Duplex MIMO Communications ● DSP Architecture for Wireless Communications ● Large-Scale MIMO Systems ● Compressive Sensing ● Network Beamforming ● Cognitive Radio Networks ● Many-Core, Multi-Core, and SoC ● Image and Video Coding ● Computer Arithmetic ● Wireless Video Transmission ● Game Theory in Communications ● Medical Image Analysis ● Coding Theory for the Next-Gen Storage Systems ● Compressive Estimation ● Multiuser and Massive MIMO ● Social Networks ● Sequence and Genome Analysis ● Low Power ● Network Optimization ● Security ● Consensus Based Algorithms ● Wireless Full Duplex ● Decoding and Detection ● Interference Alignment ● Image and Video Classification … and more

2012 Plenary Talk: "Compressive Sensing: 8 Years After," Prof. Richard G. Baraniuk, Rice University

Half-Day Tutorial: "Coding Methods for Emerging Storage Systems" – Prof. Lara Dolecek, UCLA, and Prof. Anxiao (Andrew) Jiang, Texas A&M

Save $250 through Oct. 15th.

For more information, and to register, visit:

www.asilomarssc.org

CALL FOR PAPERS

ISQED 2013

14th International Symposium on

QUALITY ELECTRONIC DESIGN

March 4-6 , 2013

Techmart Center, Santa Clara, CA, USA

www.isqed.org

Paper Submission Deadline: Oct. 12, 2012
Acceptance Notifications: November 24, 2012
Final Camera-Ready paper: January 10, 2013

Papers are requested in the following areas:

A pioneer and leading multidisciplinary conference, ISQED accepts and promotes papers in following areas:

- **System-level Design, Methodologies & Tools**
- **FPGA Architecture, Design, and CAD**
- **Design of Embedded Systems**
- **Advanced 3D ICs & 3D Packaging, and Co-Design**
- **Robust & Power-conscious Circuits & Systems**
- **Emerging/Innovative Device Technologies and Design Issues**
- **Design of Reliable Circuits and Systems**
- **IP Design, quality, interoperability and reuse**
- **Design Verification and Design for Testability**
- **Physical Design, Methodologies & Tools**
- **EDA Methodologies, Tools, Flows**
- **Design for Manufacturability/Yield & Quality**
- **Effects of Technology on IC Design, Performance, Reliability, and Yield**

Submission of Papers

The guidelines for the final paper format are provided on the conference web site. Paper submission must be done on-line through the conference web site at **www.isqed.org**. In case of any problems email isqed2013@isqed.org. ISQED papers are published in IEEE Xplore.

CALL FOR PAPERS

IEDEC 2013

Interdisciplinary

Engineering Education Conference

March 4-5 , 2013

Techmart Center, Santa Clara, CA, USA

www.iedec.org

Abstract Submission Deadline: Oct. 12, 2012
Acceptance Notifications: November 24, 2012
Final Camera-Ready paper: January 10, 2013

Papers are requested in the following areas:

IEDEC accepts and promotes papers in following areas:

- **Latest Educational Hardware and Software Tools and Techniques**
- **Advanced and Innovative Design Automation Tools**
- **Exploring the Increasing Role of Engineering in our Life**
- **Promoting Innovation and Creativity in Engineering Design**
- **Management of Design**
- **Trends in Engineering Education**
- **International and Global Aspects of Engineering Education**
- **Student Projects and Internships**
- **Learning Environments, Tools, and eLearning**
- **Combining Teaching and Research**
- **E-learning and E-assessment,**
- **Continuing Education & Its Delivery**
- **Collaboration Between Universities, Industry, and Government**
- **Engineering Education & Women**
- **Distance Learning and Distance Teaching**
- **Engineering Education Outreach**

Submission of Papers

The guidelines for the final paper format are provided on the conference web site. Paper submission must be done on-line through the conference web site at **www.iedec.org**. In case of any problems email info@iedec.org. IEDEC papers are published in IEEE Xplore.

NEW EVENT in 2012

CASE

Complex Aerospace Systems Exchange

September 11-13, 2012

Pasadena Convention Center

This dynamic, engaging event tackles some of the most important system development issues facing aerospace chief engineers, program managers, and systems engineers today, such as minimizing cost overruns and delays and mitigating late test failures. Participants will have the opportunity to hear insights, best practices, and lessons learned from recognized practitioners in each of these areas.

Three Tracks:

Complex Systems Development: Large system development activities from the establishment of requirements through the conceptual, preliminary, and detail design phases.

Integration, Test and Verification of Complex Systems: Strategies for design, mature models, databases, simulations, and test equipment to support program needs that extend from bench testing of prototypes through flight testing on multiple ranges.

Program Management to Achieve Robust and Resilient Systems: Managing the technical and direct-support aspects in the development and operation of complex aerospace systems.

Sessions: ● Forensic Investigations: Problems Rooted in Design; Problems Rooted in Program Issues ● Elegant Design and Complex Systems Development ● Planning and Executing an Integration Test Strategy for a Complex Aerospace System ● Execution of Successful Programs ● Integration of Modeling and Simulation, Ground Test and Flight Test ● New Paradigms for Complex Systems Development ● New Acquisition and Regulatory Approaches ● Verification and Validation Issues ● Business Operations and Logistics ● Complex Systems Development ● Lessons Learned in Integration, Test, and Verification ● Workforce Issues

CASE is co-located with the **AIAA SPACE 2012 Conference & Exposition.** These events will complement each other, sharing some plenary sessions and networking activities such as luncheons and receptions. By registering for CASE, you can also attend AIAA SPACE sessions at no extra cost.

Save, through August 13th!

Visit **www.aiaa.org/case**

IEEE Professional Skills Courses

Consulting Skills for Engineers: How to Become a Trusted Advisor

- Date/Time: Tuesday, August 14, 9:00AM-5:00PM
- Location: TIBCO Software, Palo Alto
- Fee: $400 for IEEE Members; $500- non-members

A unique program designed to help engineers elevate the perceptions that others hold of them beyond technical experts and into the realm of "trusted advisors" with skills that will tremendously impact your productivity and career development.

5 Habits of Intentional Leadership

- Wed-Thurs, Sept 12-13, 9:00AM-5:00PM
- Location: Synopsys, Sunnyvale
- Fee: $625 for IEEE Members; $700 non-members

Learn to identify your own leadership strengths and areas to improve; build collaboration, teamwork and trust; strengthen the ability in others to outperform; communicate your core leadership values.

SCV Chapters, Technology Management & Components, Packaging and Manufacturing Technology Societies

Communicating Across Cultures

- Thurs, October 11, 9:00AM-5:00PM
- Location: TIBCO Software, Palo Alto
- Fee: $400 for IEEE Members; $500 non-members

A "must" if you collaborate in a global team, serve customers/suppliers abroad, or work with culturally diverse H1B professionals. Learn how people from different cultures approach relationships with managers and team members, reach commitments, view initiative, accept accountability and share information.

Upgrade your skill set – prepare for future challenges

For complete course information, schedule, and registration form, see our website:

www.EffectiveTraining.com*

December 3-7, 2012
Disneyland Hotel, Anaheim

IEEE GLOBECOM is the Premier Event for telecommunications industry professionals and academics from companies, governmental agencies and universities around the world, with a technical program focused on recent communication research and development. GLOBECOM includes 12 symposia conducted by the various ComSoc technical committees covering major industry technologies and numerous hot topics – over 1000 presentations.

Keynote Presentations:

- **Vint Cerf, Google:** "Internet Challenges 2012-2020"
- **Henry Samueli, CTO, Chairman, Broadcom**
- **Krish Prabhu, President, AT&T Labs, CTO, AT&T**
- **Hossein Eslambolchi,** "The Power of Technology to Transform the Future"

Technical Sessions over 160 sessions across 12 Symposia tracks, including sessions on:

● Green Hardware and Chip Designs ● Energy Saving in Communication Network and Equipment ● Multimedia Quality of Service ● Compressed Sensing ● Theoretical Aspects of Communication Systems ● Femto-Cell Networks ● Network Coding ● Security in Cloud Computing and Storage ● Network Layer Modeling and Design ● Optical Spectrum Management ● Cognitive Radios Networks ● Spectrum Sharing ● Interference Management ● MIMO Systems ● Satellite & Space Communications ● Traffic Control ● Network Design and Management ● … and many more – see Program!

Technical Tutorials Twelve half-day tutorials

● Intro to Small Cell Wireless Networks ● Mobile-Station and Base-Station Cooperation ● Interference Alignment ● Gigabit Wireless LAN (IEEE 802.11ac) ● Content Delivery Acceleration ● QoS Provisioning in Wireless Cognitive Radio Network ● M2M in Smart Grid & Smart Cities ● Resource Management in Mobile Cloud Computing ● Opportunistic Communication ● Security Investigation on 4G LTE Wireless Networks ● Cooperative Spectrum Sensing: From Fundamental Limits to Practical Designs ● Joint PHY-MAC Design for Spectral- and Energy-Efficient Wireless Networks

22 Full-Day Workshops *selection:*

● Heterogeneous and Small-Cell Networks ● Smart Devices ● Broadband Wireless Access ● Green Internet of Things ● Machine-to-Machine Communications ● Unmanned Autonomous Vehicles ● Radar and Sonar Networks ● Wireless Cloud Computing ● Multicell Cooperation ● Optical Wireless Communications … and more

Theme:

"The Magic of Global Connectivity"

GLOBECOM INDUSTRY FORUM & EXPO – FOR WORKING ENGINEERS!

GLOBECOM, features an exposition of key providers of technology and tools, including Components, Subsystems and Systems, Test Equipment, Hardware, Software, and Middleware. The Industry Forum includes a Welcome Reception and twelve 2-hour forum sessions with broad interest programming, focused on the telecommunication industry's current practiced technology, major technology implementations, complex IT business systems, regulatory impact assessments, economic models, and engineering methods used by industry practitioners.

Disneyland Hotel

The Disneyland Resort Hotel is located steps away from the Disneyland and California Adventure parks. It is packed with fabulous dining and unexpected delights. At select times, Disney Characters are available to meet and greet Guests in the Disneyland Hotel main lobby. Bring your family! Register for your hotel room by November 2, to assure our conference rates.

GLOBECOM Early Registration Deadline:

November 2, 2012 – Save $125!

For Advance Program and registration information:

www.IEEE-GLOBECOM.org

To exhibit at GLOBECOM this year, in Anaheim, please contact Frank Chang, Tel: 1-805-218-9796, or email:

ychang@vitesse.com

CONFERENCE

Sunday-Thursday, Nov. 11-15

Sunday: Tutorials

Monday-Thursday: Technical Programming with Intermixed Tutorials

ENRICH YOUR CAREER AND FURTHER THE INDUSTRY AT THE 38TH INTERNATIONAL SYMPOSIUM FOR TESTING AND FAILURE ANALYSIS (ISTFA), NOVEMBER 11-15 IN PHOENIX, ARIZONA.

ISTFA™ is the best venue for learning new failure analysis techniques, solutions and enterprise for success.

Acquire the latest knowledge from the field's leading professionals with intermixed tutorials, short courses, technical presentations, panels, and user groups. Research leading-edge instruments and solutions at the industry's largest dedicated equipment exposition. Meet and network with hundreds of your peers from around the world. All this makes ISTFA your best opportunity to learn, network and advance your career.

Register before October 1 for early bird specials.

Go to **www.istfa.org** for up-to-date information and to register.

NEW INTERMIXED TUTORIAL FORMAT

A full day of tutorial sessions Sunday with cutting edge topics related to current trends in failure analysis intermixed throughout the week.

- Lab Management
- Electrical and Yield
- Technology Specific FA
- Package and Physical Analysis Challenges
- Fault Localization
- Microscopy
- FIB

23 TECHNICAL SESSIONS INCLUDING PANEL DISCUSSION: FA CHALLENGES OF 3D INTEGRATION

- Emerging Concepts and Techniques
- Fault Isolation and Failure Analysis of 3D Packages
- Nanoprobing Techniques/Applications
- Fault Isolation and Failure Analysis of TSVs
- Photon Based Techniques: An Understanding
- Rethinking the FA Process
- Improving Fault Isolation with Software
- Packaging and Assembly Analysis
- Counterfeit Electronics Detection and Mitigation
- Circuit Edit: Beam Interaction Studies, Strategies
- TEM Defect Detection
- Chip Level Sample Prep
- Case Studies
- Test and Diagnosis
- Device Level Sample Prep
- Alternative Energy
- Defect Analysis
- Posters

NETWORKING AND SOCIAL EVENTS

- Attendee Luncheons
- Networking Reception
- *Tools of the Trade Tour* - Registration is required
- *Hitting a Home Run with your Failure Analysis* – Inside the Diamondbacks' Chase Field
- Dessert Reception and Poster Session

TECHNOLOGY-SPECIFIC USER GROUPS

Meet, share ideas, and discuss relevant issues in a noncommercial environment. Planned topics are:

- Nanoprobing
- Focused Ion Beam
- Contactless Fault Isolation
- Sample Preparation

EDUCATION SHORT COURSES

7 Pre- and Post-Conference Short Courses

- NEW! Photovoltaic Modules: Reliability and Test Standards
- Fault Isolation
- Counterfeit Electronic
- NEW! Failure Analyzing the Failure Analysis Process
- NEW! Electrostatic Discharge in Robotic Manufacturing Lines: Electrostatic Basics, ESD-Failure Mechanisms, Tool Risk Evaluation Methods and ESD- vs. EOS-Classification and Characterization Methods
- NEW! ESD/ Factory EOS
- Financial Management of the FA Process

2012 KEYNOTE ADDRESS

University Innovation: How Today's Academic Research Seeds Tomorrow's Commercial Breakthroughs

Trevor J. Thorton, PhD, Professor and Director of Electrical Engineering, Arizona State University

Hear first-hand the trials and tribulations faced by researchers on the road towards commercial breakthrough.

REGISTER BY OCTOBER 1 AND SAVE.

- Discounted fees for EDFAS and ASM Members.
- Non-members of EDFAS receive a one year membership with their registration.
- Group discounts available

Additional information is on the ISTFA website.

Plan and register at www.ISTFA.org.

EXPOSITION - NOV. 13-14

The ISTFA exposition is North America's largest tradeshow of FA-related equipment and services. This promises to be an exciting year on the show floor where you will see the latest industry advances and network with vendors for problem-solving advice. Bring your questions, needs and concerns. Get solutions to your FA problems!

NEW in 2012!

- *Tools of the Trade Tour* – See the latest products and services in action
- Photo Contest
- Networking Reception on the show floor
- "Video Street Beat" – Coverage of your booth by editors of AM&P and EDFA magazines

The ISTFA exposition is your once-a-year opportunity to access the innovators, influencers, and decision makers –all in one location!

To exhibit, sponsor or advertise, contact Kelly Thomas at **Kelly.Thomas@asminternational.org** or 440.338.1733.

ASM INTERNATIONAL® The Materials Information Society

Everything Material®

www.istfa.org

Metro Area Workshop -- an intensive learning environment

IEEE Career Strategy and Smart Tech Professional Workshop

Friday and Saturday, September 28-29, 2012

Santa Clara Convention Center

This **Smart Tech Workshop** offers parallel, all-day track sessions that allow attendees to immerse themselves in a given technology. Below you will find the agenda and course description for each track. Attendees may choose one full-day track on each day of IEEE Smart Tech.

Friday, September 28

Three tracks run concurrently all day, choose one:

Track 1: **Embedded Software**
Morning Session: iPhone Apps
Afternoon Session: Android and Embedded Linux

Track 2: **Life Sciences**
Morning Session: Biotechnology
Afternoon Session: Medical Devices

Track 3: **Career Assistance**
Morning Session: Career Strategy Workshop
Afternoon Session: Hirable for Life

Saturday, September 29

Three tracks run concurrently all day, choose one:

Track 1: **Consulting and Patents**
Morning Session: The Professional Consultant
Afternoon Session Intellectual Property and Patents
Afternoon Session Becoming a Patent Agent

Track 2: **21st Century Infrastructure**
Morning Session: The Internet of Things
Afternoon Session: The Cloud, Big Data, Virtualization, Analytics

Track 3: **Career Assistance**
All Day: Networking and Job Seeking Skills

For full topical outlines of all Tracks, please see the complete descriptions on the website.

Who should attend?

Practicing engineers and technical professionals who are innovators, have a desire to learn more, are facing a career transition or considering a career change.

Sponsors

The Workshop is brought to you by your three Bay Area Sections and by Region 6 of the IEEE.

In the movie "The Graduate", Dustin Hoffman was told that the future was "Plastics". If the movie were made today, the guy at the party would say "Apps". *Track on Embedded Software*

The biomedical industry represents the intersection of engineering, technology, and medicine…. The industry in California is one of the largest employers and provides numerous opportunities for engineers. *Track on Life Sciences*

Specific actions experienced engineers and scientists can take to maintain, and enhance, their global competitiveness … a proven path to maintaining their competiveness throughout their careers. *Track on Career Assistance*

How you are perceived by others (prospects, clients, decision-makers, internal stakeholders) directly affects your ability to close and maintain profitable business. *Track on Consulting*

Security, privacy, data warehousing, augmenting reality through the use of intelligent agents and improving the human condition are all features of the IoT… There's no stopping the coming of massive machine-to-machine communications.
Track on 21st Century Infrastructure

Big Data is in the form of data sets that are difficult to store, manage and analyze using traditional relational databases… Often heavily unstructured, this data can stream rapidly from websites, thus requiring an expensive hardware and software infrastructure. *Track on 21st Century Infrastructure*

Workshop Fee

- $159 IEEE members
- $209 non-members
- Includes breakfast, lunch both days, evening reception Friday, keynotes

For more information, and to register, visit:

www.R6-MAW.com

Not an IEEE Member yet? As a special incentive for non-members, if you choose to pay the non-member fee – then wait and join IEEE onsite at the Workshop – you will receive a **$50 credit** toward your first-year membership dues in lieu of the member discount on your registration fee.

Sponsored by the Santa Clara Valley Section of IEEE

IEEE Senior Member Grade Elevation Night

Date: Monday, September 10, 2012

Time: 6:15 – 8:00 PM (drop in at any time between 6:15 PM and 7:30 PM)

Location: Cogswell Polytechnical College, Board Room

1175 Bordeaux Drive, Sunnyvale, CA 94089

Refreshments will be provided

The IEEE Santa Clara Valley Section, in conjunction with PACE, is sponsoring a **Senior Member Grade Elevation night** for all SF Bay Area IEEE members who meet the requirements for grade elevation to Senior Member. The requirements are posted at:

www.ieee.org/membership_services/membership/senior

Summary:

* be an engineer, scientist, educator, or technical executive in IEEE-designated fields;
* have been **in professional practice** for:
  - **7 years** if you hold a baccalaureate degree in an IEEE-designated field;
  - **6 years** if you hold a baccalaureate and a masters degree;
  - **5 years** if you hold a doctorate
* show professional maturity and "significant performance" over a period of at least five of those years in professional practice.

IEEE members who meet these requirements are **encouraged to attend.** Potential Senior Members will have an opportunity to meet with Senior/Fellow Members and possibly obtain the references that are required for the application, as well as to get a formal Nomination from the Section.

Please download the **Application Form** (**www.ieee.org/web/membership/senior-members/application.html**), enter your background/ answers and **bring 4 copies**, but do NOT begin the application process on the IEEE website (this is done AFTER our meeting). Also, members are asked to **write a few sentences** on Page 2 of the Application, or else in a file on the flash memory device, explaining how they have significantly performed their professional duties for at least five years.

To help our volunteer Senior/Fellow members evaluate your application, particularly the sections on Professional Experience and Significant Performance, please prepare a **Curriculum Vitae (CV) / resume** that contains details that don't "fit" into the application; the CV also contains details that explain possible questions that arise in the minds of the reviewers. Bring 4 copies of this resume.

Please remember that this collaborative exploratory process does not guarantee that you will receive all of the requisite references.

For any questions, please send email to John Berg **ieeenano@gmail.com**

Become a Senior Member -- See you there!

SCV Vehicular Technology, with Nanotechnology

WEDNESDAY August 29, 2012

Automated Transit Networks

Speaker: Eugene Nishinaga, CEO/CTO, Transit Control Solutions, Inc.
Time: Networking, Pizza and Drinks at 11:30AM, Presentation at 12:00 Noon
Cost: none for IEEE Members; non-IEEE Members $5
Place: TI Auditorium (Bldg E), 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: ewh.ieee.org/r6/scv/vts

Eugene Nishinaga has over 35 years experience in the design of control technology for driverless fixed guideway systems. Most recently he was the Chief Technical Officer for CyberTran International, Inc. He was employed at the Bay Area Rapid Transit District (BART) for 25 years and was the Manager of the District's Research and Development Division for 17 years. As manager of an R&D Division for a transit operation, his areas of technical involvement have included advanced energy storage devices, high temperature superconducting cable applications, artificial intelligence-based diagnostic systems, active noise cancellation, fare collection technologies, nondestructive testing, and advanced control systems. Prior to his position at BART, Eugene was employed at the Boeing Aerospace Company where he designed control circuits for the Morgantown Personal Rapid Transit in West Virginia and also software/hardware systems for the Advanced Group Rapid Transit R&D program for the Urban Mass Transit Administration. Eugene is a graduate of the University of California Berkeley with a Bachelor's degree in electrical engineering and computer sciences.

Automated Transit Networks, which are systems of driverless vehicles running on fixed track ways with all stations located off of the main line, are poised to become a major component of the transit terrain. With offline stations, traffic throughput is no longer inhibited by station platform operations so high traffic densities can be achieved with the appropriate control technology. Being able to thus operate with smaller cars, future transit service lines will be buildable for a fraction of the cost of today's heavy rail systems. Furthermore, with the ability to be powered by electricity delivered via the track infrastructure, a totally fuel-free form of transportation will be the result. This talk will discuss the potential and the challenges of such systems.

SCV Technology Management

THURSDAY September 6, 2012

Management Myths and Time Span Inconsistencies

Speaker: John Berg, BA Industries, Inc.
Time: Networking at 6:00 PM; Forum at 6:30 PM; Dinner at 7:15 PM; Presentation at 7:45 PM
Cost: $14 for IEEE members; $17 for others
Place: Ramada Silicon Valley, 1217 Wildwood Ave, Sunnyvale
RSVP: not required
Web: www.ieee-scv-tmc.org

John Berg is Chair at Vistage International, the world's leading Chief Executive Organization, with over 15,000 CEO's and business owners in 16 different countries. He is the CEO of BA Industries, Inc., which does hardware intellectual property development and monetization. Mr. Berg is the Chief Technologist at American Semiconductor, where he is developing and producing radiation-hard CMOS and memory products. Before joining ASI, Mr. Berg was a Managing Director at Cypress Semiconductor, where he grew the Programmable Logic Business Unit from $35MM to $72MM through the introduction of new programmable product families. Prior to Cypress, Mr. Berg was Vice President of Technology Development at Zilog, where he built the company's 200mm wafer fabrication facility, directed Z8 product design, and managed the scaling of CMOS and non-volatile memory technologies.

Mr. Berg did engineering and business graduate work at Stanford University, where he was a Sloan Fellow, and earned a Masters of Science degree in Management from the Graduate School of Business. He received a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology. Mr. Berg is on the Board of several privately held businesses in Silicon Valley.

In the hopes of filling a position in the corporate organization chart, we diligently interview, do personality testing and check references. We hire the person with the best of intentions only to find them failing after a few short weeks. We select our top performer and promote them to the next level, introduce them to the team as their new leader, only to find them floundering and earning no respect. You just promoted Sally -- she is now in your office complaining that her new boss has his head in the clouds and is completely out of touch with the real problems facing the department. Ten minutes later, Sally's boss, Joe, is in your office complaining about Sally, his new direct report, saying that she is totally incompetent and cannot see the big picture. What did we miss?

John Berg will discuss a set of statistically significant scientific findings of a little-known psychologist who discovered a correlation between workers across industries and their ability to handle different levels of mental complexity. Particular areas that will be discussed are:

* The flat organization is a misguided management fad -- organizational hierarchy is important and exists for very specific reasons
* A hiring manager will not willingly hire anyone at or above his or her level of mental complexity
* Personality conflicts in an organization are usually smokescreens for a deeper reason why we should not have Sally report to Joe
* Most CEOs have difficulty understanding the true nature of executive work and often, are drawn into activity that pulls them away from higher-level responsibilities.

The take-aways to this talk are the understanding of the missing link in:

* most hiring processes
* reporting relationships
* defining appropriate levels (complexities) of work

SCV Grads of the Last Decade (GOLD)

SATURDAY September 8, 2012

Woodside Hike, Huddart County Park

Coordinator:
Time: Gather at 10:00 AM at park entrance
Cost: none (there's a $6/car parking fee)
Place: Huddart County Park, San Mateo County
RSVP: not required
Web: bahiker.com/southbayhikes/huddartdean.html

Come out for a nice hike with your fellow GOLD members in San Mateo County! There is a $6 per car charge in the park, but a free parking lot close by from which we can carpool.

SCV Life Members

MONDAY September 10, 2012

Virtual Worlds: Technology, Imagination and the Future of Play

Speaker: Nanci Solomon, Xulu Entertainment
Time: Networking at 6:00 PM; dinner at 6:45 PM; Presentation following
Cost: $20.00 per person, includes buffet dinner
Place: Michael's at Shoreline, 2960 Shoreline Blvd., Mountain View
RSVP: by 5 PM Wed Sept 5th from website
Web: www.ieee4life.org/SCV

Nanci Solomon, CEO of Xulu Entertainment, has more than 25 years' experience in developing media, entertainment, and technology ventures. Xulu, the company she co-founded with her husband Jim Solomon, has developed an online physics-based virtual world along with creation tools for novices to build their own places, games, experiences, and extend the world. She's been actively involved in virtual worlds, avatars, gaming, and simulation since 1995 including co-developing a pioneering pre-broadband virtual world. It was story-based and incarnated as a real-world venue with multi-screen windows, gaming tables, motion pods, touch-screens, and other intuitive and fun natural human interfaces.

Prior to Xulu, she was VP of Marketing for Smart Machines, a robotics company (acquired by Brooks Automation). She's founded two media start-ups including a college consumer company that helped lead to the formation of Xulu, and ASIC Technology & News, where she created an award-winning magazine, executive conferences, market research, and a trade show. She was an industry analyst at Dataquest, researching and reporting on implications and applications for new technologies, and led computer-aided-design training and marketing communications at Fairchild ASIC Division.

The continued march of Moore's Law, combined with developments in software and human interface devices, has enabled a new generation of immersive virtual worlds. The introduction of new creation tools will allow novice end users to create their own physics-based virtual environments, and easily harness this technology to unlock their imagination. These online playgrounds, seamlessly tied together, will be inhabited by avatars including robots, creatures and virtual humans and filled with adventures, sports, social activities, games, and places of wonder. As interactive entertainment moves towards rich living breathing 3D worlds that will soon approach the richness of Avatar, some interesting forms of play and discovery are in store.

This presentation will include the slides, videos, anecdotes and more.

MONDAY September 10, 2012

Silicon Convergence: Creating System Solutions with Coarse- and Fine-grained Programmable Hardware

Speaker: Ty Garibay, Altera Corporation.
Time: Networking/Refreshments at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: Cadence, Bldg 10, 2655 Seely Ave, San Jose
RSVP: from website
Web: sites.ieee.org/scv-cs

Ty Garibay is the Vice President of Engineering for Embedded Processing at Altera Corporation. Previously, Ty was the Director of IC Engineering for the OMAP division in the Wireless Business Unit of Texas Instruments and was responsible for the development of TI's OMAP mobile application processors from architecture specification to production silicon. In the more distant past, he spent almost 20 years designing microprocessors of many kinds, including low-power ARM and MIPS, and high-performance x86, MIPS, 68K and 88K. Ty holds over 30 patents in the areas of computer architecture, circuit design, design methodology and design for test. Ty received his BSEE and BA Foreign Languages from Southern Methodist University in 1986.

While continuing semiconductor miniaturization enables ever more complex systems, the cost and complexity of system innovation becomes increasingly out of reach. A standard solution consisting of high performance processors, hardened peripherals, and a programmable logic fabric is ideal to address system integration challenges. Complementary to similar advances in software, a host of hardware design tools and high-level programming methodologies are also making system design more user-friendly. Together these industry advances allow design teams to flexibly implement any system to achieve the sweet spot of performance and power dissipation according to team capabilities.

In his talk, Ty Garibay will share Altera's view on silicon convergence, the integration of SoC and FPGA, and the direction the company is taking to increase system design efficiency through the use of high-level design languages and tools.

TUESDAY September 11, 2012

Smart Grids, Worse Power Quality, and Conducted 2kHz-150kHz EMC: Practical Experience Around the World

Speaker: Alex McEachern, Power Standards Lab
Time: Networking/light dinner at 5:30 PM; Presentation at 6:30 PM
Cost: Small fee for food; complimentary coffee/snacks
Place: LeCroy, 3385 Scott Blvd, Santa Clara
RSVP: not required
Web: ewh.ieee.org/r6/scv/emc

Alex McEachern is well known for his cheerful, thought-provoking speeches, and he regularly speaks at national and international conferences on electric power quality. He is the president of Power Standards Lab in California, the founder of BMI, the former president of both BMI and Electrotek, and the author of everything from the Electric Power Measurements chapter of the Encyclopedia of Electrical and Electronics Engineering to the industry-standard Handbook of Power Signatures. Active in drafting and approving international power standards, Alex is the chairman of the International Electrotechnical Commission (IEC) TC77A Working Group 9, which sets the standard for power quality instruments. He also participates in the drafting of the voltage dip immunity standards, IEC 61000-4-11 and IEC 61000-4-34. He is a Senior Member of the IEEE, former Chairman of IEEE 1159.1, a co-author of IEEE 519 and IEEE 1459, and a voting member of the IEEE Standards Coordination Committee on Power Quality. Among all his accomplishments, McEachern is proudest of the fact that companies that he has created have been responsible for over 2,400 man-years of employment. He is a reasonably inventive fellow, with 30 U.S. patents awarded so far.

As utilities start to implement Smart Grids around the world, utility specialists are recognizing that smart grids make power quality worse. This is good news for EMC engineers. At the same time, problems with conducted emissions in the 2kHz-150kHz range are popping up, often associated with smart meters. New standards are under way on measurement and immunity in this difficult frequency range - again, good news for EMC engineers. It's going to keep us busy!

WEDNESDAY September 12, 2012

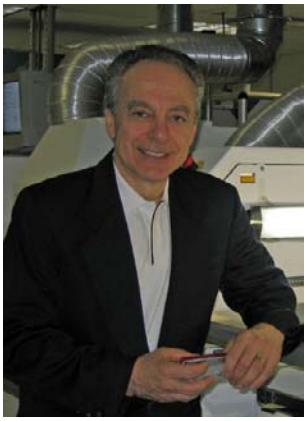
Additive Manufacturing -- It's Not Always Rapid and It's Not Just for Prototypes

Speaker: Arthur L. Chait, CEO, EoPlex
Time: Optional dinner at 6:00 PM; Presentation (no cost) at 6:45 PM
Cost: $20 for dinner ($10 for students, unemployed)
Place: Biltmore Hotel, 2151 Laurelwood Rd, Santa Clara
RSVP: from website
Web: www.cpmt.org/scv

Arthur Chait joined EoPlex as its first CEO in 2003 and became Chairman in 2004. He raised the first round of VC funding with Draper Fisher Jurvetson and Labrador Ventures. Mr. Chait recruited and hired the senior management team and acquired the company's first customers. He raised two additional funding rounds with the original investors plus ATA and Draper Richards for a total of $21 million. Mr. Chait is the key contact with investors, customers, shareholders, the press and other stakeholders. He led his team in developing new technology, and delivering prototypes to global customers. Under his direction, EoPlex has won five awards for "clean-tech" innovation. In 2009, Mr. Chait focused EoPlex on the market need for a new type of semiconductor package. This resulted in a breakthrough clean-tech product that provided lower cost and superior performance in a $4 billion/year market. In January 2012 Mr. Chait managed the acquisition of EoPlex by the Singapore Company ASTI. EoPlex has moved manufacturing to Asia and is currently building a plant in Malaysia.

Mr. Chait holds a BS degree in Engineering from Rutgers University, where he was Editor of the college magazine and a member of the Keramos honor society. He later earned an MBA in Marketing from the University of Pittsburgh in the evening program. He is a recipient of the Steinmetz Medal from GE Corporation. Mr. Chait served on the Boards of Blue Iguana Networks, MatriDigm Corp. and TechVenture Networks and is currently a board member of EoPlex. A dynamic speaker, Mr. Chait has delivered keynotes and presentations for professional societies and organizations in many parts of the world.

Producing a part in real-time with a rapid prototyping machine is magical to watch. The popular media loves to speculate about future scenarios where a consumer will be able to purchase and download a device and have it produced, Star Trek-fashion, in this way. Unfortunately dissimilar materials like silicon, wiring, glass, metal and plastic required very different processing parameters and present challenges for rapid prototyping that may never be overcome. In the meantime, there is a class of additive manufacturing that is not as flashy, but is being used for actual high-volume manufacturing. In this presentation, Arthur L. Chait, CEO of EoPlex Inc. will illustrate some examples of semiconductor parts, micro antennas, and other products that are being produced by additive processing.



SCV Circuits and Systems

WEDNESDAY September 12, 2012

2D to 3D MOS Technology Evolution for Circuit Designers

Speaker: Alvin Loke, AMD Inc.
Time: Networking/Light Dinner at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation accepted for food
Place: QualComm, Building B, 3165 Kifer Road, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/cas

Alvin Loke (S'89-M'99-SM'04) received the BASc (Eng. Physics) degree with highest honors from the University of British Columbia in 1992, and the MSEE and PhDEE degrees from Stanford University in 1994 and 1999 respectively. He was recipient of the UBC Chancellor Entrance and Canadian NSERC 1967 Graduate Scholarships. While at Stanford, his research focused on copper interconnects with low-K polymer dielectric. He has interned at Texas Instruments, Motorola, and at Sumitomo Electric Industries. From 1998 to 2001, he worked on CMOS technology integration at HP Labs, Palo Alto, and then at Chartered Semiconductor Manufacturing, Singapore as an Agilent assignee . In 2001, he transferred to Fort Collins, CO, where he designed CMOS phase-locked loop circuits for low-jitter embedded SerDes I/O and ASIC core clocking.

In 2006, he joined Advanced Micro Devices where he is currently a Principal Member of Technical Staff designing high-speed links and addressing analog/mixed-signal concerns for next generation CMOS. Dr. Loke has authored 38 publications and holds 12 US patents. He presently serves on the CICC technical program committee, SSCS Chapters committee, and ECE Department Industrial Advisory Board at Colorado State University. He is presently the SSCS Webinar Taskforce Chair, a Guest Editor for the IEEE Journal of Solid-State Circuits, and a SSCS Distinguished Lecturer.

Despite increasing economic and technical challenges to scale CMOS, we continue to witness unprecedented performance with 22-nm fully-depleted tri-gate devices now in production. This tutorial offers a summary of how CMOS device technology has progressed over the past two decades. We will review MOS device and short-channel fundamentals to motivate how device architectures in production have evolved to incorporate elements such as halos and spacers, mechanical strain engineering, high-k dielectric and metal gate, and fully-depleted fins. We will also examine key process technologies that have enabled the fabrication of these devices.

SCV Professional Activities Committee for Engineers (PACE)

WEDNESDAY September 12, 2012

Career Networking Night: Employers and Job-Seekers

Time: Pizza/drinks at 6:00 PM; networking with employers until 9:00 PM
Cost: none
Place: Ramada Inn, 1217 Wildwood Avenue, Sunnyvale
RSVP: from website (for job-seekers, for employers)
Web: sites.ieee.org/scv-pace/upcoming-events/ieee-scv-pace-career-networking-event

Special instructions for employers: please see the website. We encourage you to participate.

This is a networking event you cannot miss if you are interested in today's job market. Are you tired of looking through countless openings on company websites? Wouldn't it be great if you could meet the employers face to face and learn about the latest job openings and requirements? Do you want to stand out as a candidate and get your resume noticed or even get it to the top of the pile? If yes, then come and join us for this hiring-focussed networking night. At registration, please provide a link to your Linkedin profile and a job title for the kind of opportunity you are most interested in. We will update details on the participating employers shortly.

IEEE Santa Clara Valley(SCV) Section's Professional Activities Committee for Engineers (PACE), promotes the professional interests of IEEE's U.S. members and provides a mechanism for communication of members' views on their professional needs. Activities include Technical Training courses, Workshops on career issues (networking, career planning, career transitions, personal financial planning); skill training workshops (entrepreneurship, effective speaking, technical writing), and Government Policy as it affects Engineering and Technology.

Be sure to sign up for the Metro Area Workshop, which has a strong set of one-day workshops on getting and staying employed. Visit:

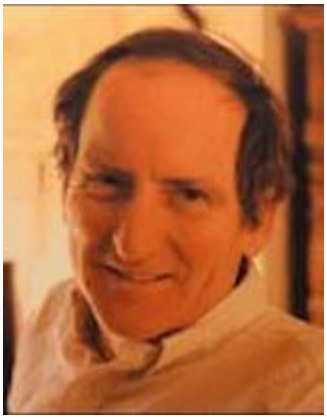
www.r6-maw.com

SCV Magnetics

TUESDAY September 18, 2012

Microwave-Assisted Magnetic Recording

Speaker: Dr Mike Mallary, Western Digital Corp.
Time: Networking and pizza at 7:00 PM; Presentation at 7:30 PM
Cost: none
Place: Western Digital, 1710 Automation Parkway, San Jose
RSVP: not required
Web: ewh.ieee.org/r6/scv/mag



Dr Mike Mallary received the S.B. degree in physics from the Massachusetts Institute of Technology in 1966, and the Ph.D. degree in Experimental High Energy Physics from the California Institute of Technology in 1971. He was a post doctoral fellow at the Rutherford Laboratory from 1972-1974 and an Assistant Professor of physics at Northeastern University from 1974-1978. There he participated in an experiment at Fermi Laboratory that produced early evidence for the fifth quark using a 300 ton solid iron magnet. From 1978 to 1980 he worked at the Magnetic Corporation of America designing large superconducting magnetics.

In 1980 he joined the Digital Equipment Corporation's effort to produce thin film heads for disk drive recording as a head modeler and designer. Here he invented the Shielded Pole perpendicular recording head which has demonstrated superior performance over the conventional monopole head and is presently in all shipped disk drives. He also invented the Diamond inductive head which doubles the effective number of turns and contributed to the theory of flux conduction in thin film heads.

Through a series of acquisitions beginning in 1992, Dr Mallary worked for Quantum, MKQC, Maxtor, and Seagate. He is presently a Senior Technologist with Western Digital Corporation. He has authored and co-authored 92 issued U.S. patents (140 total) and 52 publications. He is an IEEE Fellow and was an IEEE Distinguished Lecturer in 2009.

Perpendicular Magnetic Recording, PMR, will soon reach its superparamagnetic limit. Shingling the write process will allow significant increases in areal density but with significant system complexity and performance issues in some applications. At this time, Heat Assisted Magnetic Recording and Bit Patterned Media are the primary candidates to replace PMR. However there are significant concerns associated with these approaches. The economics of BPM are a considerable barrier by most estimates. The high temperatures of HAMR are a serious reliability concern and perfecting FePt media is very challenging. Even though MAMR is not expected to extend areal density as far as these other alternatives, its implementation would require smaller changes from PMR. Therefore MAMR may be able to sustain areal density growth while these alternate technologies are being perfected. But can MAMR be made to work well enough?

At this time there are no published demonstrations of MAMR at high densities. However, there are a number of reported observations of partial and full switching of PMR like media with moderate DC fields assisted by rf fields from micro-loops or a Spin Torque Oscillator (STO). These results will be discussed along with the results of simulations and experiments by the author. Micromagnetic simulations of the MAMR write process indicate that MAMR could approximately double recording density beyond the limits of PMR on optimized media. The system studied was that of a STO in the write gap of a wide track shielded pole PMR like head as originally proposed and patented by Prof. Jimmy Zhu of the Data Storage System Center at Carnegie Mellon University. Micromagnetic simulations of the MAMR write process, M-H loops with rf fields, Ferromagnetic Resonance of media, and STOs will be presented. In addition, some experimental results on media FMR and STO performance will be discussed.

TUESDAY September 18, 2012

Discovery and Development of Improved Scintillation Detector Materials for Medical Imaging and National Security

Speaker: Dr. Stephen Derenzo, Lawrence Berkeley National Laboratory
Time: Presentation at 7:30 PM
Cost: none
Place: Lawrence Berkeley Lab Building 55 Room 117, Berkeley
RSVP: Reservation requests to Bill DeHope, dehope1@llnl.gov are required in advance (before noon on 9/17), No Exceptions!
Web: www.mindspring.com/~banchero1/ieee

Stephen E. Derenzo is a Senior Scientist at the Lawrence Berkeley National Laboratory, Head of the Radiotracer Development and Imaging Technology Department in the Life Sciences Division, and Professor-in-Residence in the Electrical Engineering and Computer Science Department at UC Berkeley. He and his colleagues constructed two pioneering positron emission tomographs (PET) and developed advanced scintillation detectors for PET that provide high spatial resolution, depth-of-interaction information, and compact integrated circuit readout. For the past 24 years he has lead a search for new heavy scintillators and currently heads a project for the discovery of scintillation detector materials that uses automation to increase the rate of synthesis and characterization. He has authored or co-authored over 200 technical publications, seven patents, and one textbook. He has received two awards from the IEEE Nuclear and Plasma Sciences Society: the Merit Award in 1992 and the Radiation Instrumentation Outstanding Achievement Award in 2001. He became an IEEE Fellow in 2000.

Inorganic scintillators have been an essential tool of the physical sciences for over 100 years and during that time many new materials have been discovered, developed, and put into widespread use. Nonetheless there are many applications where the performance of available materials falls far short of what should be possible. These include gamma-ray stopping power and timing resolution in positron medical imaging, gamma-ray energy resolution for the identification of radioactive materials in national security, and low cost. This talk will review the current efforts in understanding the fundamental limits of detector materials, the use of empirical and first-principles calculations to guide the selection of new candidates, and the use of high-throughput synthesis and measurement techniques to discover new high-performance scintillators. The talk will be followed by a tour of the high-throughput synthesis and scintillator characterization labs and the crystal growing facility. This project maintains the largest open-access database of inorganic scintillation properties at http://scintillator.lbl.gov.

SCV Consultants' Network of Silicon Valley

TUESDAY September 18, 2012

Beyond Virtualization: A Novel Software Architecture for Complex Multi-Core SoCs

Speaker: Jim Ready, Cadence Design Systems
Time: Presentation at 7:00 PM
Cost: none
Place: KeyPoint Credit Union, 2805 Bowers Ave., Santa Clara
RSVP: not required
Web: www.CaliforniaConsultants.org

Called "arguably the one individual most responsible for establishing the embedded OS and tools market" by LinuxDevices.com, and "an iconic figure within the IT industry" by SD Times, **Jim Ready** is currently Chief Technology Advisor, Software & Embedded Systems, at Cadence Design Systems.

As the co-founder of Ready Systems, he developed the world's first commercially viable real-time operating system (RTOS) product: the VRTX real-time kernel. Ready Systems, founded in 1980, merged with Microtec Research in 1993, went public in 1994, and was acquired by Mentor Graphics in 1995. During this period, Jim served as Ready Systems' President, and as chief technical officer (CTO) at Microtec/Mentor.

Jim invented the category of embedded Linux commercialization in 1999 when he founded MontaVista Software where he served as CEO and later CTO. In 2009, MontaVista was acquired by Cavium, a leading SoC supplier for the networking and telecommunications market. After the acquisition, Jim continued to serve as CTO for MontaVista until he joined Cadence in May 2012.

Moore's law continues to drive the development of increasingly complex semiconductor devices, most notably the SoC (System on a Chip). However, silicon designers have now hit a significant constraint in utilizing the seemingly infinite number of transistors available to them when trying to increase processor performance: they have reached a point where they are limited by the power consumption (and heat) generated by simply increasing clock speed to gain performance.

In response, the industry has embarked upon a disruptive change by increasing performance through processors composed of multiple computing cores, essentially turning to parallel computing as the new performance driver. In addition, certain computing environments use an additional "trick" to increase system performance by adding application-specific hardware offload engines along with multiple computing cores to accelerate overall SoC performance.

Both of these approaches have significant implications for both the operating system and the applications running on an SoC. While the simple answer has always been to invoke the "magic" of virtualization to provide a flexible software framework for these advanced SoCs, reality says otherwise. This talk will illustrate the limits of virtualization (at least as currently available) and describe some new operating system approaches that look to provide a better fit between the advanced SoC hardware and the application software.

SCV Nanotechnology

TUESDAY September 18, 2012

Nanotechnology-Enabled Redox-Flow Batteries Give the Smart Grid a High IQ

Speaker: Dr. Craig Horne, Founder and CEO, EnerVault Corporation
Time: Registration & light lunch 11:30 AM; Presentation at 12:00 Noon
Cost: IEEE Members and Students $5; Non-Members $10
Place: Texas Instruments Bldg E-1 CMA Room, 2900 Semiconductor Drive, Santa Clara
RSVP: from website
Web: www.ieee.org/nano

Craig Horne is a renewable energy technology and start-up veteran in areas of, fuel cells, batteries, telecom, and nanotechnology. With more than 20 years of experience working with renewable energy technologies overlapping with 9 years in nanotechnology, the majority of his career has been spent in ground-level projects (synchrotron radiation spectroscopy of Li-ion materials, nanoscale material based Li-ion components, nanoscale material and processes for telecom components, disruptive manufacturing of fuel cell stacks, new system designs for flow batteries). Among others he's worked at nanotechnology firms like Nanogram Corporation, Kainos and NeoPhotonics Corporation. He has 19 US patents awarded, over 14 US applications pending, and numerous international patents. He received his Ph.D. in Material Science and Engineering, Univeristy of California Berkeley

Megawatt scale Redox Flow Batteries (RFB) can be a safe, reliable and cost effective and clean solution to utility distributed-scale energy storage. The demands of peak loading and fast EV charging are immediate applications and enabling the smart grid is on the near horizon. Nanotechnology applied to separators and chemicals is enabling this disruptive technology to be the just in time disruptive solution to a major energy storage problem. Sunnyvale's EnerVault Corporation has exploited this and is bringing fully integrated modular systems to provide an economical solution.

OEB Industry Applications

THURSDAY September 20, 2012

Combining Power System SCADA and PMCS Software into One Solution: A Hybrid Approach to Enable Power System SCADA functionality with PMCS Analysis and Energy Information

Speakers: Rick Hofstetter and Luke Dalske, Schneider Electric
Time: Social/Networking at 5:30 PM; presentation at 6:15 PM; dinner at 7:15 PM; Presentation continues at 8:00 PM
Cost: $25 for IEEE members, $30 for non-members, $15 for student and retired members
Place: Zio Fraedos, 611 Gregory Lane, Pleasant Hill
RSVP: by September 17 to Michael Nakamura, mnakamur@ebmud.com or (510) 287-2066
Web: www.e-grid.net/docs/1209-oeb-ias.pdf

Rick Hofstetter is a Business Development Specialist for Schneider Electric Energy Solutions. Rick has 23 years of experience delivering solutions for power distribution systems. He has developed collaborative relationships to provide power monitoring and energy information solutions at many of Northern California's major energy users. In 2005 Rick co-authored a paper on Load Preservation Systems that was presented at IEEE PCIC Conference in Denver. In addition, Rick has presented at several IEEE Meetings and industry conferences in Northern California.

Luke Dalske, PE, is a solution sales engineer for Energy Solutions a division of Schneider Electric. At Schneider Electric, Luke has been involved in the design, implementation, and sales of critical power monitoring applications in mission critical facilities. He has over 10 years of experience in implementing PLC and SCADA systems for the controls industry in multiple industries.

As technology has evolved, the definitions of power system SCADA software and power monitoring software (PMCS) have become less distinct. In fact, many of the features of each solution overlap with the other. This presentation will provide an overview of the key functionality of both power system SCADA software and power monitoring software. Additionally, we will review applications where each technology is used. Finally, we will present a hybrid solution where both are combined in a single power system.

The presentation will include many aspects of power system monitoring and control including network security issues, sequence of event recording and timekeeping, ways to leverage industry standard open protocols to integrate devices from multiple manufacturers into one software front end, and how to get the most value from your power quality meter investment.

WEDNESDAY September 19, 2012

Underwriters Laboratories (UL) Tour

Speaker: Mr. John Taecker, PE, senior engineer, UL
Time: Social/Snacks/Drinks/Desert at 5:15 PM; presentation and tour at 5:30 PM
Cost: none
Place: UL, 455 East Trimble Road, San Jose
RSVP: required, from website
Web: meetings.vtools.ieee.org/meeting_view/list_meeting/13171

John Taecker, P.E., has worked for Underwriters Laboratories for over 27 years. He has a BS in Mechanical Engineering from Cal Poly, San Luis Obispo, and is a California Registered Professional Engineer in Safety Engineering. He is a nationally recognized speaker on electrical, building, mechanical, and plumbing products and installations. He serves on the IAEI Southwestern Section Board of Directors, and is an Inspector Member of the International Association of Electrical Inspectors (IAEI), and a Professional Member of the International Code Council (ICC) and the International Association of Plumbing and Mechanical Officials (IAPMO).

Join us for an informative tour of UL's Northern California laboratory located on the corner of Trimble Road and Junction Avenue in San Jose. Types of products tested at this facility include high technology (information technology equipment, EMC), Health Sciences, industrial equipment (power and controls), wire and cable, and consumer appliances (e.g. lighting and HVAC). The tour will also include an opportunity to learn about other services UL provides, and how to readily find information about UL certifications.

Due to security reasons, attendance is limited to max of 35 on first come first serve basis. Please make sure to reserve your spot using the link indicated on your left.

This is a joint meeting between the Oakland East Bay Power and Energy Society and the International Society for Automation (ISA), Northern California Section.

SCV Grads of the Last Decade (GOLD)

SATURDAY September 22, 2012

High-Impact Interpersonal Communications: How to Communicate with Anyone, Anywhere – and Get More Results with Everyone, Everywhere

Instructor: Stuart Friedman, Global Context
Time: 8:30 AM - 1:00 PM
Cost: IEEE Members $30; non-members $40 by Sept. 8th. (Save more -- bring a friend!) Includes continental breakfast and lunch
Place: Qualcomm Cafeteria, 3165 Kifer Road, Santa Clara
RSVP: from website
Web: www.ieee-scv-gold.org

Possessing strong Interpersonal communication skills in today's business environment is every bit as important as your technical abilities. Join SCV GOLD for a 4 hour seminar, you will learn to have more effective conversations with everyone you encounter, and eliminate misunderstandings.

You'll begin communicating your messages – both verbally and written in a more persuasive manner. By knowing how to adapt your own communications style to fit the specific situation, you'll start building trust and rapport with those you previously thought impossible.

Stuart Friedman is an electronics engineer, having held roles in engineering, sales/mktg, executive, business development and consulting. He has a longtime professional interest in communication within engineering organizations.

THURSDAY September 27, 2012

The Origins of Silicon Valley: Why and How It Happened Here

Speaker: Paul Wesling, IEEE SF Bay Area Council Communications Director
Time: Lunch at 11:45 AM; Presentation at 12:15 PM
Cost: $15 for lunch ($5 for students, unemployed)
Place: Biltmore Hotel, 2151 Laurelwood Rd, Santa Clara
RSVP: from website
Web: www.cpmt.org/scv

Paul Wesling has worked at GTE, Amdahl, Tandem Computers, H-P and several start-ups, in R&D, design, and manufacturing technology. Assignments included bubble memory development, IC packaging, multi-chip modules, thermal management, reliability, and executive management, as well as developing advanced technology and professional skills courses for the technical staff. A Fellow of the IEEE, he received the IEEE Centennial Medal, the CPMT Distinguished Service award, and the IEEE's Third Millennium Medal, and served as the CPMT Society's vice president of publications for 22 years. Now retired, he is communications director for the IEEE's SF Bay Area Council and the editor of the Council's GRID Magazine.

Paul has served the local Santa Clara Valley CPMT chapter since 1972, as an officer and more recently as Chapter Advisor. His enthusiastic and inventive approach to volunteer organizational development was honed in the Boy Scouts, both as a youth (he's an Eagle Scout) and as a Scoutmaster of a troop of 60 to 100 Scouts for 15 years. Through his initiative and oversight, the SCV CPMT Chapter has put on over 450 multi-evening and full-day classes locally, making the chapter financially independent and setting its reputation as a high-service-delivery unit of the IEEE. The chapter earned the Society's Best Chapter award twice during his service, and has organized a number of the Society's conferences, including IEMT and SEMI-THERM.

He earned his BS-EE and his MS-Materials Science, both from Stanford University. He holds the Extra Class Ham radio callsign KM6LH. From his career in Silicon Valley, he has had a clear view of the developments here over the past 4 decades.

Why did ***Silicon Valley*** come into being? The story goes back to local Hams (amateur radio operators) trying to break RCA's tube patents, the sinking of the Titanic, Naval ship communications requirements, Fred Terman and Stanford University, local invention of high-power tubes (klystron, magnatron), WW II and radar, William Shockley's mother living in Palo Alto, Hetch Hetchy water, and the SF Bay Area infrastructure that developed -- these factors pretty much determined that the semiconductor and IC industries would be located in the Santa Clara Valley. And since semiconductor device development and production were centered here, it made sense that Charles (Bud) Eldon of H-P would be asked by his management to start an IRE Group on Component Parts in Palo Alto, to serve our local engineers (which grew into today's CPMT Society).

Paul Wesling, a CPMT Society Distinguished Lecturer, will give an exciting and colorful history of device technology development and innovation that began in San Francisco, moved down the Peninsula (seeking lower costs and better housing), and ended up in the Santa Clara Valley during and following World War II. You'll meet some of the colorful characters -- Lee DeForest, Bill Eitel, Charles Litton, David Packard, Bill Hewlett and others -- who came to define the semiconductor and IC industries through their inventions and process development.

SATURDAY September 29, 2012

Weekend Workshop: Next Generation Circuits & Systems, Communications and Sensor Technologies in Mobile Devices

Speakers: Prof. Tom Lee, Stanford; Prof. Roger Howe, Stanford; Prof. Viktor Gruev, Washington U; Theodore Yu, TI; Prof. Debbie Senesky, Stanford; Steve Lloyd, InvenSense; Jay Esfandyari, STMicroelectronics; Harmeet Bhugra, IDT
Time: 8:30 AM to 4:45 PM
Cost: $30 for IEEE members, $40 for others (includes lunch -- $10 more after Sept. 22)
Place: Edward J. Daly Science Center, Santa Clara University, Santa Clara
RSVP: from website
Web: ewh.ieee.org/r6/scv/comsoc or ewh.ieee.org/r6/scv/cas

High Resolution and Real-Time Polarization Imaging Sensors by Viktor Gruev, Department of Computer Science and Engineering, Washington University in St. Louis, St. Louis, MO.

Solid state imaging devices now dominate the multi-billion dollar industry of digital photography. These typically capture two properties of light, namely the intensity and the wavelength, and encode this information into perceptual quantities of brightness and color. The third property of light, polarization, has been ignored by solid state imaging sensors partially due to the human inability to discriminate polarization information.

In this talk Prof. Gruev will present a novel imaging sensor capable of capturing the polarization properties of partially polarized light in high resolution and in real-time. The imaging sensor monolithically integrates aluminum nanowire optical filters with CCD imaging array to achieve a high resolution polarization imaging sensor.

Prof. Gruev will also present several applications that take advantage of the high resolution and real-time sensing of polarization information. These applications range from underwater imaging of polarization phenomena in marine species, to tracking of vehicles in urban environment and endoscopic imaging of mouse heart tissue.

(***continued***, *next page* ➔ ➔)

This workshop covers advances in MEMs based sensors and the continuing progress in the integration of these sensors with control, signal processing and communication electronics. Several of the speakers will also address end-user solutions (motion characterization, contextual awareness, gestures, sensor-aided navigation, haptic feedback, health and fitness, life-logging, etc.) which illustrate what can be achieved with the availability of these sensing interfaces (Accelerometer, Proximity, Touch, Pressure, Camera etc) on a connected platform.

After a keynote talk by Professor Tom Lee, we will have two themes. The first (morning) theme focuses on progress in the development of circuits, sensors and devices whereas the second (afternoon) theme covers advances in hardware and identifies applications/usage scenarios. Each session is approximately 2 hours and 30min duration including keynotes and Q&A. The attendees will also have an opportunity to interact with vendors at the tabletop exhibits. There will also be an opportunity to review projects from Santa Clara University's Center for Science, Technology, & Society at this workshop.

Workshop Speakers:
Keynote: Prof. Tom Lee, Stanford University

Morning: Progress in Circuits, Sensors & Devices
Morning Keynote: Prof. Roger Howe, Stanford
Speaker 1: Prof. Viktor Gruev, Washington Univ
Speaker 2: Theodore Yu, Texas Instruments
Speaker 3: Prof. Debbie Senesky, Stanford

Lunch & Networking

Afternoon: Hardware & Applications
Afternoon Keynote: Steve Lloyd, VP of Engineering, InvenSense
Speaker 1: Jay Esfandyari, MEMS Market Development Manager, STMicroelectronics
Speaker 2: Harmeet Bhugra, Managing Director, MEMS Group, IDT Inc.
Speaker 3: *Being confirmed.*

Event-based Analog Sensing by Theodore Yu, PhD, Texas Instruments

The event-based sensing approach encodes features of interest from the environment or scene into events. Incorporation of low-power analog signal processing locally near the sensor seeks to reduce the amount of redundant data processed in the system. Furthermore, encoding of relevant features into time-stamped events allows for additional signal processing techniques that naturally exploit the temporal dynamics of the sensed information. Dr. Yu will first present some work that implements event-based sensing techniques for visual and acoustic sensors. The second part, he will cover the design and implementation of an event-based processor modeled after the dynamics of the brain. Within this architecture Dr. Yu will demonstrate spike-based event-driven coincidence detection in neural synchrony with applications towards temporal encoding and decoding of scenes.

Progress in Extreme Environmental Sensing Using Wide Bandgap Semiconductor Thin Films by Prof. Debbie G. Senesky, Stanford University

In this presentation, Prof. Senesky will discuss the synthesis of temperature tolerant, chemically resistant, and radiation-hardened wide bandgap semiconductor thin films and nanostructures. These new material sets serve as a platform for the realization of sensor, actuator, and electronic components that can operate and collect data under the most hostile conditions. More specifically, smart and adaptable structures for extreme environments are enabled through the technology developed in her laboratory. Her research efforts support a variety of applications including deep space systems, hypersonic aircrafts, combustion monitoring and subsurface monitoring.

Track-2 Keynote: **CMOS-MEMS Integration will be a Requirement for the Next Generation "Smart" MEMS Sensors** by Stephen Lloyd, VP of Engineering, InvenSense

In years past, many of the attempts at CMOS-MEMS integration have had marginal results. Consequently, many of today's leading high volume MEMS suppliers use separate MEMS and CMOS processes and leverage advanced packaging to combine the two die into a single package. There are significant challenges in combining MEMS with CMOS, yet once these challenges are overcome, a CMOS-MEMS platform offers a significant advantage for implementing highly integrated "smart" sensors. Verified by the evolution of CMOS technology, integration is an extremely powerful tool to lower overall solution cost and power. CMOS-MEMS integration achieves similar significant advantages in cost, size, and power consumption over solutions with separate MEMS and CMOS. This discussion will cover the challenges of CMOS-MEMS integration and demonstrate how effective solutions to these challenges exist and are in high-volume production today. We will discuss the advantages of a CMOS-MEMS platform for many applications such as inertial, audio, ultra-sonic, timing, RF, biological, chemical and gas sensing. The talk will also briefly cover a CMOS-MEMS platform that is available via a fabless design model (NF Shuttle) where silicon is manufactured at leading foundries.

Emerging Multi-sensor Modules and Sensor Fusion Enables New Applications by Jay Esfandyari, MEMS Market Development Manager, STMicroelectronics

MEMS based sensors hold a distinct edge over other technologies in performance, size, cost and current consumption. These advantages have enabled the strong penetration of MEMS sensors into high growth applications in portable devices.

Multi-sensor based applications such as indoor navigation, motion gaming, robot balancing, image stabilization, air mouse, human body tracking and unmanned aerial vehicles, etc. require the fusion of the data of these sensors to achieve high performance and short response time.

This presentation will give an overview of which sensors are used in sensor fusion, what the major technical parameters are required and what the most popular applications of the sensor fusion solution are. It will also discuss the challenges the developers are facing and the limitations associated with the sensor fusion implementation.

Introducing World's first Piezoelectric MEMS Oscillators by Harmeet Bhugra, Managing Director, MEMS Group, Integrated Device Technology, Inc.

Mr. Bhugra will discuss the introduction of world's first high performance piezoelectric MEMS oscillators. These non-quartz oscillators are gradually penetrating the $4B frequency reference marketplace and are increasingly being favored by system designers. He will discuss major application trends and address why alternative solutions to quartz are gaining traction. He will also discuss what it takes to get a MEMS product from paper to production including key lessons learned during development.

THURSDAY October 11, 2012

Mini-Symposium: ESD Troubleshooting Techniques for Electronic Designs; Fundamentals of Signal and Power Integrity

Speakers: Doug Smith, D. C. Smith Consultants, and Prof. Ege Engin, San Diego State University
Time: Registration/breakfast at 7:30 AM; instruction from 8:30 AM - 5:00 PM; reception following
Cost: $250 for IEEE Members; $275 non-Members; $100 Students/Unemployed (includes lunch)
Place: Biltmore Hotel, 2151 Laurelwood Rd, Santa Clara
RSVP: from website
Web: ewh.ieee.org/r6/scv/emc

Doug Smith held an FCC First Class Radiotelephone license by age 16 and a General Class amateur radio license at age 12. He received a B.E.E.E. degree from Vanderbilt University in 1969 and an M.S.E.E. degree from the California Institute of Technology in 1970. In 1970, he joined AT&T Bell Laboratories as a Member of Technical Staff. He retired in 1996 as a Distinguished Member of Technical Staff. From February 1996 to April 2000 he was Manager of EMC Development and Test at Auspex Systems in Santa Clara. He currently is an independent consultant specializing in high frequency measurements, circuit/system design and verification, switching power supply noise and specifications, EMC, and immunity to transient noise. He is a Senior Member of the IEEE and a former member of the IEEE EMC Society Board.

Dr. Ege Engin received his Ph.D from the University of Hannover, Germany. From 2005 to 2008, Dr. Engin was with the Packaging Research Center at Georgia Tech, where he was an Assistant Director of Research. Previously, he was with the Fraunhofer-Institute for Reliability and Microintegration (IZM), Berlin. Since 2008, he is an Assistant Professor in the Electrical and Computer Engineering Department of San Diego State University. He has more than 80 publications in journals and conferences in the areas of signal and power integrity modeling and simulation and three patents. He is the co-author of the book "Power Integrity Modeling and Design for Semiconductors and Systems," published by Prentice Hall in 2007. Dr. Engin is the recipient of the Semiconductor Research Corporation Inventor Recognition Award in 2009.

ESD Troubleshooting Techniques for Electronic Designs

Tracking down the sources of ESD problems in equipment can be difficult in modern electronic designs. After a brief overview of the characteristics of ESD and its effects on equipment, simple and effective troubleshooting techniques will be discussed that Mr. Smith has developed over many years of solving ESD problems. Live demonstrations will be used to illustrate some of the techniques.

Fundamentals of Signal and Power Integrity

As the clock frequencies for off-chip signals approach 20 GHz and beyond, maintaining signal and power integrity are becoming major issues to design a computer system that can actually support such speed. This mini-symposium will cover fundamentals of modeling, simulation, and characterization techniques to ensure signal and power integrity. The following topics will be covered in this tutorial:

Session 1: Power integrity modeling and design
Session 2: Signal integrity modeling of losses
Session 3: Advanced topics: Modeling of through silicon vias for 3D ICs; power plane filtering using electromagnetic bandgap structures.

Reception & Exhibits: 5:00 PM - 6:00 PM

There will be an exhibition by vendors of EMC design, test and measurement products and services. During the reception in the exhibit area, heavy appetizers and beverages will be available. You are welcome to attend the reception only at NO CHARGE, provided a registration form is submitted in advance. Thus, if you can't join us for the entire day, drop by for the reception and exhibition to network with the speakers and attendees as well as vendors. You might even win a raffle prize! Anyone who ONLY wishes to attend the Reception & Exhibits must register. The Reception & Exhibits session is also organized as a PACE (Professional Activities Committees for Engineers) event under IEEE-USA.

SCV and OEB Life Members

SATURDAY October 13, 2012

Motivating Our Students to Become Engineers: How You Can Make It Happen

Speakers: Dr. Peter Staecker, 2012 IEEE President-elect, and others
Time: Registration at 8:30 AM; seminar from 9:00 AM - 1:00 PM
Cost: none
Place: Santa Clara County Education Office, 1290 Ridder Park Dr, San Jose
RSVP: from website
Web: www.ieee4life.org

PROGRAM FEATURES:

Opening remarks by **Dr. Peter Staecker**, 2012 President-elect of the IEEE.

An eye-opening presentation by the former Superintendent of a South Bay School district to discuss the problems of California public schools.

Speakers representing the following groups will tell us how retired volunteers can help students to regain America's technical leadership:

- TOPS (Teaching Opportunities for Partners in Science)
- RE-SEED (Retiree Enhancing Science Education through Experiments and Demonstrations)
- IEEE TISP (Teacher In-Service Program) by Michael Lightner, IEEE VP of Educational Activities

Concurrently, in the same building a K-8 teacher conference will explore ways to incorporate technology into their teaching. Some of those teachers will also speak to us about their goals and needs. You'll have opportunities to talk with the teachers and the IEEE officers during lunch.

California, next to last?

In the United States, California K-8 students in math and science rank – 49th!

US students rank 19th and 24th among the industrialized countries of the world!

- Research shows those who don't learn basic math in early grades will struggle with algebra.
- Kids whose interest isn't sparked in science won't consider a career in engineering.
- Kids weak in basic math and science who DO enter engineering schools drop out.

Who will develop the transistors, circuits, systems, high-speed trains and low-emission cars of the future? Who will find practical energy sources, solve the environmental problems and construct protection against global terrorism? If the present trend of poorly prepared American students continues, who will bring back America's technical leadership?

Without an adequately educated population, America's top schools can't provide enough engineers for the US to solve the technical challenges of the 21st Century. China and India are graduating far more engineers than the US. If the trend continues, American companies will be forced to outsource even their design work.

The Santa Clara Valley and Oakland/East Bay IEEE Life Member Groups are offering an opportunity to explore ways to assist K-8 teachers' effectiveness. Who better to inspire K-8 students in technical careers than our IEEE Life Members? By showing youngsters that engineering can be an exciting and important profession, veteran engineers can assist teachers in the classrooms to generate enthusiasm for the basic skills.