



GSPx 2005

Pervasive Signal Processing Conference and Expo

Oct 24 - 27, 2005 • Santa Clara Convention Center • Santa Clara, CA USA



KEYNOTE SPEAKER

"Broadband Wireless Opportunities and Challenges"

Dr. Andrew J. Viterbi

Pioneer in Wireless Communications,
Co-founder of QUALCOMM and
creator of the Viterbi Algorithm



KEYNOTE SPEAKER

**"Signal Processing Catches the
Multicore Wave: Which Architecture
is Right for Your Application?"**

Dave Mothersole

Chief Technology Officer, Networking and
Computing Systems Group and Director of
Advanced Technology Development,
Freescale Semiconductor



KEYNOTE SPEAKER

"Mobile OFDMA for Triple Play Services"

Dr. Rajiv Laroia

CTO of QUALCOMM's OFDMA
division (former CTO and founder
of Flarion, acquired by QUALCOMM)

**Signal processing has become the technology driver for the entire
electronics industry...because it is the basis of our mobile
communications and multimedia future.**

— Will Strauss, Industry Analyst, President, Forward Concepts

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TUTORIALS

New Tutorials will be added. Be sure to visit www.gspix.com and check back often for updates.

• VIDEO COMPRESSION

MICROSOFT CORPORATION VC-1

DR. SRIDHAR SRINIVASAN, WINDOWS CORPORATION, DEVELOPMENT LEADER OF WINDOWS MEDIA CODECS GROUP

- This tutorial is an introduction to the VC-1 bitstream format, and is intended for a diverse audience. First, we look at the Windows Media ecosystem, the relationship between the VC-1 format and its embodiment WMV9. We present an architectural overview of VC-1 and describe its various functional blocks. We also discuss standardization issues. In the next part of the tutorial, we consider aspects of implementation of the VC-1 decoder including profiles & levels, as well as computation issues. We examine blocks that may require optimization. We wind up this discussion with a look at the conformance requirement and post processing for visual quality improvement.
- In the third part, we look at an implementation of a VC-1 encoder. We list all the degrees of freedom provided by the bitstream and study their usage. We provide a guideline for implementers who must decide which features to support in a phased manner. We also discuss rate control issues, panic and special modes as well as optimization and pre processing.
- In the final part of the tutorial, we provide an overview of the steps involved in putting together a VC-1 enabled end-to-end system. Here, we briefly cover WMA and WM-DRM, together with transport issues and a look at Microsoft porting agreements, support offerings and roadmaps.

H.264/MPEG-4 AVC CODER

DR. MARTA KARCZEWICZ, SENIOR RESEARCH MANAGER, NOKIA RESEARCH CENTER

- History of the development of the MPEG-4 AVC standard.
- Brief comparison of MPEG-4 AVC with previous standards.
- Detailed discussion of new Video Coding layer elements: context-adaptive variable-length coding (CAVLC) and context-adaptive binary arithmetic coding (CABAC), in loop deblocking filter, exact-match transform coupled with quantization matrix, directional, spatial domain intra prediction, motion compensation and prediction utilizing variable block sizes, multiple reference frames and quarter-sample accuracy. Costs and benefits of each tools will be considered - impact on coding efficiency versus impact on complexity.
- System integration of H.264/AVC codec.
- New standardization initiatives: Scalable Video Coder (SVC), Multi-View Video Coding and H.265.

VIDEO COMPRESSION IN SURVEILLANCE: A CASE STUDY OF THE CITY OF LONDON

PETER FRY, DIRECTOR OF THE CCTV USER GROUP, UK

• WIRELESS

WIMAX

MR. NAFTALI CHAYAT, CHIEF SCIENTIST, ALVARION

The tutorial will cover the WiMAX and the underlying IEEE802.16 standard. The first part of the tutorial will focus on the WiMAX for the Fixed Wireless Access applications, while the second will cover the underlying principles of Mobile Broadband Access based on 802.16e standard.

Part 1

- Market background of WiMAX
- Principles of OFDM and upstream OFDMA
- Principles of 802.16 MAC
- Support of Advanced Antenna Systems in 802.16

Part 2

- Mobile WiMAX - market background
- OFDMA based physical layer
- AAS and MIMO extensions
- 802.16 MAC extensions for mobility
- Summary

UWB AND ZIGBEE

PATRICK KINNEY KINNEY CONSULTING LLC ; CHAIR, IEEE 802.15 TG4A; COVICE CHAIR, IEEE 802.15; CHAIR, ZIGBEE GATEWAY WG

This tutorial will cover wireless technologies from the ZigBee Alliance and also Ultra Wideband (UWB) initiatives such as WiMedia, Wireless USB, and UWB Forum as well as the standards efforts behind these technologies.

Part 1 ZigBee Alliance

- Market background
- Overview of Network layer
- Overview of Application Support Layer
- Description of the IEEE 802.15.4 PHY and MAC
- Competing technologies such as Z-Wave, etc.
- Summary

Part 2 UWB

- Principles of UWB
- Regulatory environment of UWB
- Market background of multimedia
- Alliances within multimedia UWB: WiMedia, Wireless USB, and the UWB Forum
- Overview of IEEE 802.15.3a standards effort
- Market background of ranging/location awareness
- Overview of IEEE 802.15.4a standards effort

ADVANCES IN WIRELESS LOCAL AREA NETWORKS -LAN AND MIMO

DR. BENNY BING, ASSOCIATE DIRECTOR OF THE GEORGIA TECH BROADBAND INSTITUTE, EDITOR IEEE WIRELESS COMMUNICATIONS MAGAZINE

- Topic 1: Introduction to wireless LANs, including its evolution, standards and evolving technologies.
- Topic 2: Fundamentals of Wireless LAN Design and Deployment covers radio spectrum trends, physical layer transmission, MAC protocols, network topologies, security, switches, and deployment considerations (e.g., office, home, public hotspots/hotzones).
- Topic 3: 802.11 Wireless LAN Standards summarizes current 802.11 standards.
- Topic 4: Emerging 802.11 Standards discusses new 802.11 initiatives focusing on high-speed MIMO systems (802.11n), intelligent wireless systems (802.11k), wireless mesh networks (802.11s).

• MULTI-CORE PROCESSORS

BENCHMARKING MULTI-CORE PROCESSORS BASED ON PROCESSING THROUGHPUT

DR. WINTHROP (WIN) W. SMITH, ENGINEERING FELLOW RAYTHEON COMPANY, LEADER IN MULTI-CORE PROCESSOR CHIP & BOARD/BOX LEVEL

Focused look on Multi-core Processors. From architecture to implementation to software development through 5 key lectures and sessions on Multi-Core Processors Chip and Board/Box Level. Sessions with the participation of:

- Analog Devices
- Codito Technologies
- Hewlett Packard
- IBM Blue Gene Group
- IBM Cell Processor Group
- IBM Power Pc Group
- IMEC
- Intel Itanium Group
- Intel Xeon
- GEDAE
- Mirabilis Design
- Philips Silicon Hive Processor

• SYNTHETIC APERTURE RADAR IMAGERY

CUTTING EDGE MULTI-DIMENSIONAL SAR IMAGE EXPLOITATION TOOLS FOR REMOTE SENSING, SURVEILLANCE AND TARGET DETECTION

DR. CHRIS OLIVER, CBE, LEADER IN SAR IMAGING

These lectures are directed towards the fundamental physical principles that determine our ability to extract information from SAR imagery. Many of these fundamental principles can be found in 'Understanding SAR Images', by Oliver and Quegan, now republished by SciTech (ISBN 1-891121-31-6). However, the presentations contain considerable developments of these principles undertaken over recent years. The presentations are divided into 5 lectures addressing: SAR image formation, defects and correction (lecture 1); Information from SAR intensity (lectures 2 and 3); Information from polarimetric imagery (lectures 4 and 5). The lectures will start by examining the physical basis that underlies the information, introducing suitable models to represent the data, proposing algorithms for optimal information extraction, and discussing application examples

GSPx is the only independent conference and exhibition where the signal processing community can see the latest ideas, innovations and products in a single event.

— Ken Karnofsky, Director of Marketing, The MathWorks, Inc.

TECHNICAL WORKSHOPS

New Technical Workshops will be added. Be sure to visit www.gspcx.com and check back often for updates.

MONDAY, OCT 24 • 8:30 AM – 4:00 PM

PREPARING SOFTWARE FOR MULTI-CORE PROCESSORS

Lori Matassa, Intel Infrastructure Processor Division, Intel

This workshop is focused on the task of migrating software from a single processor to a multi-processor environment, particularly addressing customers migrating to dual-core processor architectures. The first half of the workshop will peel back the onion of the software stack and explain the implications for operating systems, libraries, drivers, and tools. Strategies for maximizing performance through multi-tasking, application partitioning and application threading are compared. The basics around parallel software are presented, including how to express parallelism to software tools, determine the correctness of code, and assess the resulting code performance.

The second half of the workshop is targeted at software developers by providing a more detailed perspective on threading and scalability with respect to applications analysis, decomposition, measurement and relevant tools. Participants may elect to attend the first half or full day workshop.



MONDAY, OCT 24 • 8:30 AM – 12:00 PM

MODEL-BASED DESIGN FOR VIDEO SYSTEMS ON EMBEDDED DSPS

Model-Based Design is a complete design flow that enables developers to use a single executable model of their entire system for algorithmic exploration; system design, simulation, and visualization; implementation with automatic code generation; and testing, validation, and design verification.

In this workshop, we will apply Model-Based Design using Simulink® from The MathWorks to design, implement, and verify video applications on TI DSPs. Attendees will be exposed to all the steps of system design, including modeling, simulation, code generation, implementation on TI DSPs, and verification of the generated code in real time. Two video application examples – edge detection and video stabilization – will be used as the design examples.

We will then create models of the application in Simulink with the Video and Image Processing Blockset, simulate the model to validate algorithms, and convert the model to a fixed-point data type for embedded implementation. Using Real-Time Workshop® and the Embedded Target for TI C6000 DSPs, C-code will be automatically generated for execution on a TI C6416 DSK. The generated code will then be verified in real time, in the same environment using the Link for Code Composer Studio.



MONDAY, OCT 24 • 8:30 AM – 12:30 PM

INTRODUCTION TO MULTI-STANDARD, MULTI-CORE SYSTEM DESIGN

Are you implementing H.264 Main Profile + DVB-H + WCDMA Release 6 + WiMax WirelessMAN-OFDMA all on one chip? Even if your project contains fewer standards, multi-core processor system design is on your agenda. Specifying the application and architecture followed by programming the implemented chip can be very daunting tasks, especially if your current background is off-the-shelf DSPs or the design of dedicated hardware.

In this introductory workshop, experts from CoWare will explain the fundamentals of electronic system-level (ESL) design techniques and you will learn how to address the following aspects:

- Modeling and verification of complex applications
- Modeling, exploration and programming of complex, multi-core architectures
- Modeling, exploration and implementation of application-specific processors

CoWare will explain concepts like data flow modeling, transaction-level modeling, instruction set modeling, C-Compiler generation and how they can be applied to solve your design task at hand.

This workshop is intended for system architects, lead engineers, software programming tool developers and design managers who are interested in advancing their skills and organizations to ESL design. All examples and case studies come from CoWare's experts who help electronics companies produce differentiated products.



MONDAY, OCT 24 • 8:30 AM – 12:00 PM

HOW TO RAPIDLY DEVELOP DSP-FPGA SYSTEMS USING C-BASED DESIGN & MODEL BASED DESIGN

Steve Chappell, Celoxica Inc.

Flemming Christensen, Sundance Microprocessor Technology Ltd.

System designers commonly choose between DSP processors and FPGAs to implement complex algorithms and signal processing systems. Both technologies have their merits, but combined they offer a compelling solution based on power, perfor-



mance, flexibility and product differentiation. The traditional barrier to combining these benefits has been different design flows and different design languages.

During this interactive, technical workshop Celoxica and Sundance will present real-time DSP-FPGA design examples including image and video processing and Software Defined Radio (SDR). Targeting TI DSP and high density FPGAs, the development flow from algorithm to implementation will use Celoxica's C-based hardware design integrated with model based design using Simulink. The presenters will guide developers through the complete design flow, the selection and complimentary use of DSP and FPGA and the characteristics of board level platforms.

If you design systems, where power, performance and product differentiation are key, or if you're just curious, attend this workshop.

MONDAY, OCT 24 • 8:30 AM – 12:00 PM

RAPID PROTOTYPING WITH FPGAS: USING VERY WIDE BAND DIGITAL RECEIVERS AND ENERGY DETECTION SYSTEMS AS AN EXAMPLE



Join us for a brief discussion on using our COTS Family of PCI and/or VME base boards and I/O cards to provide Rapid Prototyping for your algorithms and systems. See how you can quickly implement and test your algorithms in real time, on real hardware, for quick and accurate results. Move to prototype more quickly to gain approval for the next stage of the project.

As an example, we will show you how to build Wide Band Digital Receivers and process an entire spectrum without decimation or data loss. We will discuss how you can program the FPGAs for energy or pulse detection at these rates using our Application Development Tool - CoreFire. This combination of off the shelf hardware and software will allow you to start collecting and processing data in the Giga Samples per second range within the first week of getting hardware. We will also discuss the COTS solutions for real time storage of the raw and processed data at the GSPS rates.

MONDAY, OCT 24 • 8:30 AM – 12:00 PM

STREAMLINING WAVEFORM PORTABILITY ACROSS FPGA ARCHITECTURES



Synplicity, Inc. (<http://www.synplicity.com>) has introduced their Digital Signal Processing development tool for Field Programmable Gate Arrays (FPGAs). The new tool, Synplify® DSP, drastically simplifies algorithm development, area/speed performance, and portability for SDR applications. When used in conjunction with their Synplify Pro® FPGA Synthesis tool, allows SDR waveform developers to take executable Simulink specifications modeled with Synplicity's blockset and produce optimized platform independent RTL code for any specified FPGA environment, regardless of the FPGA vendor. Synplicity's IP Blockset does not contain any hardware specific information, allowing modeling at the algorithmic level, while this single source executable model will be utilized for hardware implementation through a DSP Synthesis engine. This permits porting of waveform products without tedious and expensive recoding for different FPGA implementations, freeing radio designers to employ more current FPGAs later in the design/development cycle.

This tutorial will demonstrate the design of a Digital Down Converter algorithm generic to a Software Defined Radio. The implementation will show the ease of modeling using a DSP level blockset that is independent of any hardware implementation details. After modeling, the implementation will be simulated, analyzed, and then automatically implemented in an FPGA. We will then demonstrate the automatic re-targeting to a different FPGA, without any changes to the system model. The methodology includes the design and use of portable IP components. This methodology and implementation in the Synplify DSP and Synplify Pro tools, achieves that goal of waveform portability in the FPGA hardware implementation path. This approach is additionally portable to ASIC implementations.

MONDAY, OCT 24 • 1:00 PM – 2:30 PM

INTRODUCTION TO VIDEO COMPRESSION-SESSION 1 OF 2

Jeff Bier, Berkeley Design Technology, Inc., BDTi



Video compression algorithms ("codecs") manipulate video signals to dramatically reduce the storage and bandwidth required while maximizing perceived video quality. Understanding the operation of video codecs is essential for developers of embedded systems, processors, and tools targeting video applications. For example, understanding video codecs' processing and memory demands is key to processor selection and software optimization.

In this presentation, we explore the operation and characteristics of video codecs. We explain basic video compression algorithms, including still-image compression, motion estimation, artifact reduction, and color conversion. We discuss the demands codecs make on processors and the consequences of these demands.



TECHNICAL WORKSHOPS

New Technical Workshops will be added. Be sure to visit www.gsp.com and check back often for updates.

MONDAY, OCT 24 • 2:30 PM – 4:00 PM



PROCESSORS FOR CONSUMER AUDIO/VIDEO APPLICATIONS -SESSION 2 OF 2

Jeff Bier, *Berkeley Design Technology, Inc., BDTI*

Dozens of processor manufacturers offer hundreds of processors targeting consumer audio and video applications. Making a good selection is a crucial step in the product development process. Some selection criteria are obvious—for example, the processor must be fast enough for the application. But speed is not enough—the processor

must also measure up in terms of efficiency, development tools, peripherals, and other criteria. How can system developers balance these considerations?

In this presentation, we provide the background needed to select a processor for a consumer media product. We begin by exploring the types of processors used in these applications, including general-purpose CPUs, DSPs, media processors, and application-specific standard products. We characterize the strengths and weaknesses of each type of device, and evaluate leading processors in terms of performance, efficiency, development infrastructure, and vendor strategies. We present a logical, step-by-step processor-selection methodology, and highlight key trends in the rapidly changing processor landscape.

TECHNOLOGY PANELS

New Technology Panels will be added. Be sure to visit www.gsp.com and check back often for updates.

BRANDING DOWN TO THE ARCHITECTURE: STANDARD VS. CUSTOM

Moderator: Jim Turley, *Editor in Chief, Embedded Systems Programming Magazine*

Panelists: Markus Levy, *President & CEO, EEMBC (Embedded Microprocessor Benchmark Consortium)*

Dan Davis, *Director of Multimedia Solutions, ARC International*

Noam Shendar, *Director of Marketing, MIPS Technologies*

Giovanni Gozzini, *Director of Hardware Development, UPEK, Inc.*

THAT OASIS ON THE HORIZON IS NO MIRAGE

Moderator: Ed Sperling, *Editor-in-Chief, Electronic News Magazine*

Panelists: Panelists to be announced

HOW ACCELLERA STANDARDS SUCH AS PROPERTY SPECIFICATION LANGUAGE (PSL) & SYSTEMVERILOG CAN BE USED TO IMPROVE IP DELIVERY AND VERIFICATION.

Moderator: Victor Berman, *Director of Language Standards, Cadence Design*

Panelists: Harry Foster, *Chief Methodologist, Jasper Design*

Cesar Quiroz, *Scientist, CoWare*

Arturo Salz, *Scientist, Synopsys*

Cary Usery, *President & CEO, Founder Improv Design*

George Bakewell, *Director of Technical Marketing, Novas*

MULTICORE ICS – PROBLEM OR OPPORTUNITY?

Moderator: Dr. Winthrop Smith, *Engineering Fellow, Raytheon Company*

Panelists: Daya Nadamuni, *Chief Analyst & Research VP, Design & Engineering, Gartner*

Johannes Stahl, *Marketing Director, CoWare*

Mark Lippett, *CTO, Ignios*

Simon Davidman, *CEO, Imperas (previously founder & CEO of CoDesign Automation)*

Steve Krueger, *Core IP Architect, Texas Instruments*

Sven Brehmer, *CEO, Polycore Software*

THE FUTURE OF PROCESSORS FOR DIGITAL VIDEO

Moderator: Jeff Bier, *Founder and President, Berkeley Design Technology, Inc., BDTI*

Panelists: Chris Day, *General Manager and Senior Director of Marketing of Advanced Media Processing, Philips Semiconductors.*

Dr. Pat Hays, *Vice President of Engineering at MIPS Technologies.*

Joshua Kablotsky, *Division Fellow, Embedded DSP Division, Analog Devices, Inc.*

Mark Oliver, *Senior Manager of Multimedia Video Imaging Solutions Marketing, DSP Division, Xilinx*

Ralph Weir, *Director of Marketing, Elixent*

ENGINEERING OUTSOURCING

Moderator: Stephen Schuster, *CEO and Founder of Rainier Co.*

Panelists: Analog Devices, Asus, Green Hills

WHAT IMPACT WILL THE DEVELOPMENT OF ELECTRONIC SYSTEM LEVEL (ESL) HAVE ON SIGNAL PROCESSING TECHNOLOGIES?

Moderator: Jeff Jussel, *VP Marketing and Americas General Manager, Celoxica*

Panelists: Ken Karnofsky, *Marketing Director Signal Processing and Communications, The MathWorks*

Dr. Randy Allen, *CEO and Founder, Catalytic*

Farzad Zarrinfar, *VP of Worldwide Sales & Marketing, Poseidon Design Systems*

Johannes Stahl, *Marketing Director, CoWare*

Shawn McCloud, *Product Line Director for High-level Synthesis, Mentor Graphics Corporation*

Stan Krolkoski, *CEO, ChipVision*

VIDEO COMPRESSION: WHICH STANDARD WILL PREVAIL?

Panelists: Microsoft Corporation, Nokia, QUALCOMM, Texas Instruments

WIMAX & UWB MARKETING HYPE MEETS TECHNICAL REALITY

Moderator: Rosendo "Rocky" Gonzalez, *Founder and CEO, A2e Technologies*

Panelists: Ken Stanwood, *CEO of Cygnus Communication and Vice-Chair of the IEEE 802.16 Working Group,*

John Santhoff, *2005's Technology Innovator of the Year Award Recipient, Founder and CTO of Pulse Link, Inc.*

Jeff Harris, *Director at General Atomics*

FPGAS VS. PROCESSORS: WHAT'S THE RIGHT CHOICE FOR SIGNAL PROCESSING?

Panelists: Altera, Xilinx, Sundance, LYR Tech, Texas Instruments or Analog Devices

For [RF Engines], this is probably our favorite show of the year. It's well focused, in a good location and yields a good volume of sales leads. The companion conference also fits our interests really well. Although only in its second year, we feel it has a great future and we look forward to next year.

— John Lillington, CEO / CTO, RF Engines Ltd.

PAPERS

Be sure to visit www.gspc.com and check back often for updates.

AEROSPACE AND RADAR

- High Performance FPGA Computing Platform for a Closed-Loop Flight Control Turbulence Detection System
- Heterogeneous Implementation of an Adaptive Bayesian Beamformer
- Radar Processing Heterogeneous Future Technologies
- Wideband, High Resolution ADC Technique Validated by Residual Error Analysis

ALGORITHM IMPLEMENTATION

- Efficient Methodology for Implementation of Matrix Inversion in Fixed-point Hardware
- An Efficient Implementation of Canonical Minimum Redundancy Prefix Code
- Simple Implementation Solution of a General Purpose Hilbert Transformer Operating over more than Two Frequency Decades
- Reconfigurable Matrix Multiplication For Reconfigurable Devices
- A Novel Method for Jitter Separation Based on Gaussian Mixture Model

ARCHITECTURES

- Challenges in PowerPC440-FS Soft Core Development: Timing Perspective
- Using Multiple Custom Instruction Configurations to Accelerate Computation of Algorithms
- Cache Based Adelante DSP for Application Driven SOC Evolution
- A Hardware Performance Analysis Framework for Architectural Exploration of DSP Systems
- Optimized Pipelined Time Shared Real Time Machine (OPTSRM)
- Simulation Analysis of a Very Long Instruction Word Processor under Globally Asynchronous and Locally Synchronous Multi-Processor Technology with Improved Efficiency
- Dynamically Reconfigurable Hardware Design for Low Latency Time
- VLSI Architecture for Video Compression Using Hybrid Transform
- Alternatives in New Controller Designs: SoC, SIP or Distributed Processing
- The Emergence of ASIC Disruptive Technology: In - Standard Metal; Out - Standard Cell
- Fast Track Third Party IP Core Integration - An Efficient Two Pass IP-Based ASIC Design and Verification Methodology
- The StarCore SC2400 as a Mobile Application Processor Accelerator
- Design of Application-Specific Instruction-Set Processors for Multi-Media, using a Retargetable Compilation Flow
- Industry Trends and Challenges in Providing Small Form Factor (SFF) HDD Technology to the CE Marketplace
- Bringing Automation to the Verification of SoC Based Designs
- The Next-Generation Packet-Based Multi-Processor DSP
- Architectural Considerations for Multi-Channel High Speed Data Acquisition in Sensor Processing Systems

AUDIO

- An Efficient Asynchronous Sampling-Rate Conversion Algorithm for Multi-Channel Audio Applications
- Designing and Debugging Efficient, Real-Time Audio DSP Systems in a Graphical Programming Environment
- An Audio Signal Processing System for Wired and Wireless Headsets
- Voyageur: Ultra Low Power Reconfigurable DSP Platform for Personal Audio Systems
- Optimization of Ogg Vorbis I Decoder on TMS320C6x Platform
- Psychoacoustic model and audio compression
- A Development of a Vocal Suppressor with .NET Platform

AUTOMOTIVE

- Systems Software Requirements for In-Car Digital Entertainment
- When Cars Can See: How Automotive Vision Will Roll Out
- 1394-Automotive – TTP Gateway for In-vehicle Applications
- Hands Free Telephony - A Framework Based Approach
- Accelerating Automotive Video-Based Active Safety System Development with Model-Based Design
- The Digital Car - Are we there, yet?
- How FPGAs Enable Automotive Systems
- Intelligent Road Sign Detection for Vehicle Video Processing
- Simulation Analysis of Re-engineered Legacy Engine Management System
- Assisted Lane Maneuvering System using Computer Vision

BIOMEDICAL

- Effects of Detection System on Surface Detected Motor Unit Action Potentials: A Simulation Study
- Precise Segmentation of Cleavage of the Neuron Stem Cells in Time Lapse Image Sequences

- Cancer Cell Recognition by Fuzzy Logic in Medical Images
- Classification of Myoelectric Signal Patterns using an Artificial Neural Network on a Multi-function Myoelectric Controller
- QT Interval Analysis in ECG Signal and Syndrome of Sudden Death by using Kohonen Networks
- Medical Images Adaptive Compression for Transmission and Archiving Application to MRI Modality
- Positron Emission Tomography (PET)

• BIOMETRICS

- Using Software-Configurable Processors in Biometric Applications
- A Robust Fingerprint Recognition Scheme
- Student-Class Attendance Record Using Fingerprint Identification Sensor
- Fingerprint Image Enhancement using Composite Method
- Fingerprint Image Enhancement using Morphological Transform
- Face Recognition using Eigen Faces Method

BROADBAND AND DATA COMMUNICATIONS

- Fiber Optic Microcellular Network
- Implementing a FPGA-Based Broadband Modem Using Model-Based Design
- Design of POS Interface using Network Processor

CONSUMER ELECTRONICS

- 16-Bit Controllers and ISM Band Radio Application in Home Access Control
- Open Architecture Settop Box Platform
- Development of a Real-time System to Detect Audio Smoke Alarm Signals
- Secure, Low-cost On-Chip Firmware Storage for Embedded Signal-Processing Systems
- An Effective Dynamic Handoff Support for Mobile Media Network
- Mobile Navigation Movie Player: A Navigation tool based on GPS and Streaming Multimedia Player

DIGITAL FILTERS

- Computationally Efficient Architecture for the Design of QMF Bank with CSD Coefficients
- Structural Synthesis of Multiplierless Digital Filters
- Generation and Enumeration of Structures of IIR Digital Filters
- Design of Multistage Filters Using CICs
- Implementation Eighth Order IIR Filter using FPGA

DIGITAL RADIO

- Optimisation of a Scalar Sampling DRFM in an FPGA
- Flexible Architectures for Wideband SDR Channelisation
- Spectral Efficient Technologies in 3G for Packet Access
- Design Optimization of a DSSS Receiver Using Hardware Co-Simulation
- The Performance of the Modified Saturation Routing Algorithm in a Tactical Communication Network
- Software Defined Radio - Signal Processing Subsystems
- Development, Code Generation and Systems Integration
- Building Secure SCA-enabled SDR Hardware and Software

EMBEDDED SOFTWARE, SOFTWARE ARCHITECTURE AND SOFTWARE TOOLS

- A Hybrid Real-time, Secure, Operating Environment Supporting Windows and Linux
- Multilingual Compact Fonts for Digital Displays
- Power Efficiency for Real-time Embedded Systems
- How to Optimize Software Effectively in DSP Embedded Systems
- Emerging Web Technologies Needs - XML Based Rich Clients
- Coping with Algorithm Modifications During the Design Process
- A C Model for UMA3.x Architecture Evaluation
- Tool-flow For an Automated Compilation of SIMULINK and Real-Time Workshop Applications onto Heterogeneous Platforms
- Linux as an Embedded Operating System and Development Environment
- Implementing a Multi-Threading Scheduler in a Real-Time Operating System for Digital Signal Processors
- Transaction-based Debug of Communication-centric Embedded Platforms
- Understanding DSP Synthesis
- Metrics-based Behavioral Design: A Methodology for Quickly Realizing High Quality Hardware for Signal Processing Applications
- Graph Theoretical Modelling and VLSI Design Framework for Entropy Based Signal Processing Models

FPGA-BASED DSP

- FPGA Implementation of OFDM Modem
- A Comparative Study of LFSR based Pseudo Random Number Generators Implemented in FPGA
- An Efficient Communication Controller Architecture for FPGA-Based Hardware Acceleration of Signal Processing Applications
- FPGA Based Platform for High Speed Embedded Computing
- A Compact High Resolution Phase-Factor Generator for Large Point-Size FFTs
- FPGA Implementation of OFDM Modem
- Real-Time Matrix Multiplication on FPGA
- Optimization Techniques for Efficient Implementation of DSP Applications in Modern FPGAs
- FPGA Co-Processing Architectures for Video Compression
- MicroArchitectural Modifications And Determination of Parametric Dependencies For Very Large Instruction Word (VLIW) ASIP's Custom Instruction Selection
- New Sum of Absolute Differences Architecture For Motion Estimation
- Exact Bucket Sorting for Segmented Screen Rendering

IMAGE PROCESSING

- Image Compression on FPGA
- Co-efficient Folding Based Lifting Scheme for One Dimensional Discrete Wavelet Transform
- A Bayer Pattern Based Fast Color Conversion Technique
- A High-Speed Column-Based Architecture for the Coefficient Bit-Modeler of JPEG2000
- An Exponential-Model Based Pre-compression Bit Allocation Algorithm for The JPEG2000 Standard
- Disease Identification for Prevention of Calamity Using Image Processing
- Automated Self-Calibrating Detection and Removal of Blemishes in Digital Images
- VLSI Architecture of Real-time Adaptive Video Enhancement Using Wavelet Transform
- Fast Integer Arithmetic Wavelet Transform Properties and Application in the Multiprocessing Unit Real-time System
- Paradigm Shift in Development of Artificial Vision System for Blinds
- Reconfigurable VLSI Architecture Design for Real Time Image Stabilization
- Development of Gesture Recognition Based Virtual Keyboard
- Image Restoration using Discrete Periodic Radon Transform (DPRT) and Genetic Algorithm (GA)
- Neural Network based Video Object Recognition
- A Morphology Based Method for Car License Plate Detection
- Content-based Image Retrieval Based on Fuzzy Sets Theory and Learning Automation
- Automatic System for In-Camera Person Indexing of Digital Image Collections
- New Building Blocks for Computer-Based Recognition
- A Distributed Infrastructure for Person Recognition using Mobile Phones
- Medi Image System Version 4.0

INDUSTRIAL CONTROLS AND APPLICATION

- Novel Open Architecture for High Speed CNC
- Design of Genetic based Power System Damping Controller
- Integrated Neural Systems for Active Vibration Control
- Systematic Development and Test Methodology for Complex Multimedia Applications
- Creating a 'Black Box' Recorder to Trace Real-Time System Bugs
- Overcoming Bandwidth Obstacles using Crosstalk Cancellation Technology
- Signal Processing for Reduction of Noise in Electric Machines
- Robotic Soccer Image Processor (RSIP) - FPGA Implementation

MILITARY SIGNAL PROCESSING AND SYNTHETIC APERTURE RADAR (S.A.R) IMAGERY

- Radar System Instrumentation using COTS DSP
- Two New Classes of Impulse-Mpulse-Equivalent Signals and Detectors for Long Range, High Resolution, Radar and Sonar Systems Capable of Detecting Closely-spaced Stealth Aircraft, Ships, and Submarines
- COTS Signal Processing Techniques and Standards for Military Applications
- Exploiting SAR Imagery at the Sensor
- On the use of Spatial Constraints in SAR Image Segmentation
- Development of GIS Maps for Mobile Communication Applications- A GPS Based Approach

>> PAPERS CONTINUE ON NEXT PAGE



PAPERS

Papers will be added. Be sure to visit www.gspix.com and check back often for updates.

MODELING AND SIMULATION

- Design and Verification of Communications Systems using Model Based Design
- Fast Bit-Accurate C++ Datatypes For Functional System Verification and Synthesis
- Instruction Set Level and System Level Co-Verification
- A Framework for Fast Simulation of DSP Algorithms on Multiprocessors
- Building a Complex SystemC System by Reusing Legacy C++ Models
- Consolidated Modeling Approaches at the System Level Support Flexible Implementation Paths
- Design and Implementation of Embedded Motor Controllers
- Modeling and Analysis of LiNbO3 Optical Modulator with Superconducting Electrodes

MULTI-CORE/MULTIPROCESSING

- Common Programming Models with a Dual-Core Processor
- Using a Dual-core Processor in Power-Sensitive Applications
- Acceleration of Signal Processing Applications Using Parallel FPGA-Based Processing Boards
- Code Partitioning - Optimizing an Asymmetric Multi-core System
- A Framework for the Automatic Generation of Audio Processing Applications on a Dual-CPU System
- Optimizing Inter-processor Communication on Freescale i.300-30 Multi-core Platform
- A Multi-Core Architecture for In-Car Digital Entertainment
- A Multiple Core Distributed MPEG4 High Resolution Decoding Scheme on Freescale i.300-30 Innovative Convergence™ Platform
- Programmability Solution for Embedded Applications on Multi-core/multiprocessor Architectures
- Large FFTs on a Cell Processor
- Channel Decoding and Equalization with the Viterbi Coprocessor (VCOP) on the MSC8126
- Cell in Radar
- Cell Primitives
- Compiler-Synchronized Multiprocessor System Based Programmable Device
- HP presents dual core performance characterization using results from work with commonly used ISV codes, and discusses implications for optimizations and system configurations.
- An H.264 compatible video encoding algorithm on a CellProcessor
- Autocoding Sensor Processing Applications to Run on Multicore Processors
- Automation in Single Chip Parallel Programming - The "Cascade" Language
- Blue Gene/L Packaging
- Cell Broadband Engine support for privacy, security, and digital rights management applications.
- Code Partitioning - Optimizing an Asymmetric Multi-core System.
- Construction of a Parallel MPEG4 Video Decoder on a Multi-core Architecture using CASCADETM
- Delivering Scalable Software on Blue Gene/L
- Enabling Software-Programmable Multi-Core Systems-on-Chip for Consumer Applications
- Exploiting Parallelism, While Managing Complexity using Silicon Hive Programming Tools
- Gedae for Multiprocessor Systems - Implications of Multicore Processing
- Gedae Language Features for FPGA and Multicore Programming
- HP Scalable Visualization Array plans using multi-core systems and advanced graphics processing units.
- Implementing Mode Control on Multiple Processor Systems
- Life Sciences on Blue Gene
- Lilliputians of Supercomputing Have Arrived - Blue Gene/L Overview
- Multi-core and hyperthreading resource management for clusters based on work done in HP Advanced Development by an internal taskforce.
- Multi-core futures for HP platforms - roadmap for the three processors and platforms
- Multi-Core Processing Improvement Analysis for RADAR STAP Processing
- Multi-Core Systems for Digital Video Reception and Video Processing
- Rugged Embedded Clusters for DOD programs with 10G Myrinet switch fabric and FreeScale
- Server Capabilities of Intel's next generation Itanium(r) Server Processor
- Silicon Hive's Scalable and Modular Architecture Template for High-Performance Multi-Core Systems
- Technical Details of Intel's next generation Itanium(r) Server Processor
- Terrain Rendering Engine (TRE): Cell Processors Optimized Real-time Ray-caster

NETWORKING

- Access Media Gateways Pave the Way to IP
- Enhancement and Performance Analysis of Industrial Ethernet
- FPGA Implementation of High-speed Symmetric Crossbar Schedulers for VLAN Switches
- A Fuzzy Logic Based Approach for QoS Routing in Computer Network

POWER MANAGEMENT

- Topics on Power Management in Cellular Systems
- Industry Trends in Power Management Technology for the CE Marketplace
- Obtention of a Power Management Scheme for an Embedded System through Simulation
- Power Architecture for CompactPCI Platforms

PROGRAMMABLE AND PROGRAMMING DSP

- Philips Semiconductors Adelante VD32040 Architecture: An Embedded Vector Processor for Low Power DSP Applications
- LSI's ZSPFastFloat Floating Point Format and ZSPFF Coprocessor Implementations for ZSP DSP Cores
- Critical Decisions for DSP System Designers on Performance, Price Power, Peripherals
- Enabling Use of Dynamic Storage Allocation in Real-Time Embedded DSP Applications
- Analysis of Loop Behavior of Selectable Mode Vocoder and Its Impact on Instruction Level Parallelism
- High Performance DSP Programming with Embedded C
- Porting Open-source Algorithms to Advanced Digital-signal Processors
- Accelerating Compute Intensive Functions Using C and Software-Configurable Processors
- Optimization of MPEG2/4 AAC Decoder on TMS320C6x Platform
- C/C++ Loop Transformations for Hardware Synthesis
- Optimum Register and Functional Unit Assignment for VLIW DSPs: A Case Study
- Programming the ITU-TSS CRC32 Algorithm in High-speed PowerPC AltiVec Assembly Language
- Optimizing the GNU C Compiler for the TMS320C6x DSP
- A Secure, Field Upgradeable Operating System Architecture for Blackfin Microprocessors

SPEECH PROCESSING AND RECOGNITION

- Output-Based Speech Quality Assessment in Mobile Communications Using Hidden Markov Model
- Automatic Gain Control for Speech and Audio Signals
- Clustering Techniques at the Subvector Level for Discrete Mixture HMM (DMHMM) Acoustic Models
- Microphone Array Geometry for Interference Suppression with Robustness Against Inaccuracies in the Far-Field Assumption
- Improving SNR of Speech Signal by Spectral Subtraction method using Matlab and VHDL
- A Pitch Detection Based New Doubletalk Detector
- Discrete Words Speech Recognition Using Self-adaptive Hidden Markov Model (HMM)
- Implementation of SOPC Based Isolated Word Recognition System
- Isolated Word Recognition using Dynamic Time Warping
- Effect of Speech Rate on Speech Recognition Accuracy

VIDEO BROADCASTING AND PROCESSING

- Implementing a Single-Core DVB-H Player on a StarCore SC2400 Processor
- An Efficient Motion-adaptation De-interlacing Technique on VLIW DSP
- Architecture
- Implementation of Motion Estimation Algorithms on Dynamically Reconfigurable Processor
- RapidIO in Video Infrastructure Systems

VIDEO COMPRESSION AND PROCESSING

- Software and Hardware Solution for Software and Hardware Solution for H.264 Video Decoder on HDTV Applications
- Instruction and Data Cache Optimizations for MPEG4 Decoding on Freescale i.300-30 Innovative Convergence™ Platforms
- H.264 Video Encoding Algorithm on a Cell Processor
- SVEN - Scaleable Video Engine for the High Definition TV Market
- Media Processor Architectures for Mobile DVB-H Terminals
- Implementation of H.264 Encoding Algorithms on a Software-Configurable Processor
- A Low Power Soft Core for Multi-standard Video Applications
- Low-Cost Solutions for Video Compression Systems
- Scalable FPGA Design for MPEG-4 Codec Applications
- Implementation of MPEG-4 Encoder on Sandblaster

- Implementation of MPEG-4 Encoder on Sandblaster
- Realtime Optimization Techniques for Processor Based H.264 Intra Frame Compression
- Exploiting Thread-level Parallelism in H.264
- Implementation of Video Codecs using MIMD Processors
- Efficient Implementation of Video Encoder on Symmetric Multicore Processors
- A Dynamically Reconfigurable Stream Processor for Video Processing: Object-Oriented Approach using MPEG-4

VoIP

- Enabling Media Services in a VoIP Network
- Open Standards Solutions in the VoIP Communications Equipment Market
- Latency and QoS Management for Wireless VoIP
- Towards Real-Time Objective Assessment of Conversational Speech Quality for Next Generation IP Networks
- What Should You Look at Choosing your Enterprise Conferencing Tool?
- An Ultra Low-Power/Cost Cellular-VOIP and Wifi-VOIP Methodology
- A VoIP SoC Design Using ARM Core and the Implementation of VoWLAN Phone Function
- A Layered Approach to Evaluating Processor and System Performance for VoIP Applications
- Adaptive Filtering in the Presence of Additive Noise

WIRELESS COMMUNICATIONS AND TELEPHONY

- Implementing 802.16-2004 SDR Using a Software-Configurable Processor
- Beamforming Techniques for MIMO-OFDM Systems
- aacPlus in the 3GPP and 3GPP2 Context
- An Improved Algorithm to Minimize Clock Offset Effect for 4G OFDM System
- Implementation of UE Synchronization Unit for 4G OFDM System
- GSM Baseband Optimization on a Parallel Processing Architecture
- A Channel Assignment Scheme for Wideband Systems
- Ultra Wideband (UWB) - Innovative Technology
- Channel Estimation using Kalman Filter for UWB Communication Systems
- On an OFDM-UWB System with Two-Tap Adaptive Linear LMS Equalization
- Performance Evaluation of Multiband Orthogonal Frequency Division Multiplexing
- Full Rate FPGA-based Synchronization Circuit For Multiband-OFDM UWB Receiver
- VLSI Implementation of High Speed FFT Processor for UWB Multiband OFDM
- A Sub-band Based Approach to Space-Time Adaptive Processing for UWB Multi-Access Systems
- FPGA based WiMAX System Design
- S/W Implementation of High Performance 802.16 on a TigerSharc Processor
- Using Signal Processing Algorithms and RF Behavioral Models to Optimize Wireless Communication Designs
- Performance Analysis of Equalization Schemes for 802.11b Receivers
- IP Strategies in Today's Wireless Technology Revolution
- DSP Implementation of Adaptive Channel Equalizer to Overcome Intersymbol Interference in a Digital Cellular Communication
- Enhancing Data Efficiency in IEEE 802.11a using Equalization
- A Study on the Implementation of Authentication techniques for the CDMA Flight Termination System
- Simulation of Adaptive Modulation
- High Rate Turbo Equalization Based on LDGM Codes
- A Novel Channel Estimation Method for OFDM Mobile Communication Systems Based on Pilot Signals and Divided Wavelet Transform
- Air Interface Technologies for Evolved UMTS
- Adaptive Channel Estimation Techniques for OFDM Systems in Doppler Channels
- CORDIC-Based RLS Algorithm Via Systolic Array Mechanism
- Enabling New Technology Adoption into Portable Embedded Systems
- UMTS and HSDPA Implementation on the StarCore SC1400 Processor
- Satellite IP
- Multi-chip Remote File System
- Performance and Quality of Service Management in GPRS Network
- Design of CDMA Matched Filter Chip using VHDL and Implementation in Vertex Devices
- Reconfigurable Architecture for CDMA

The strength of GSPx is its focus on Digital Image and Signal Processing. GSPx 2004 was a meeting-of-minds for anyone interested in the technology and provided a combined conference and exhibition where ideas could be shared and relationships developed.

— Chris Sullivan, Director of Strategic Alliances, Celoxica Ltd.

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NEW PRODUCT FORUM TUESDAY, OCTOBER 25, 2005 – 1:00 PM

Do You Have a New Hardware or Software Product that Will Be Introduced at GSPx?
If so, we want to hear from you!

Your audience will be expo and conference attendees plus trade and business press editors.

Submissions should only be for new hardware and software products, not previously announced prior to GSPx 2005, in the areas of signal processing, DSPs, embedded applications, and EDA tools for developing signal-processing chips or subsystems.

The deadline for New Product Forum submissions is SEPTEMBER 26, 2005.

Please send your submissions, not to exceed 400 words, to Jim Lipman (ednjim@earthlink.net) and Will Strauss (wis@fwdconcepts.com) to be eligible for consideration. You may include no more than two graphics with your descriptions. We will honor embargos up to the October 25 date. Please include a contact person name, phone number and email with your submission.

We look forward to receiving your entries for the GSPx 2005 New Product Forum and hope to see you at the show!

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Sincerely,

Will Strauss
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