GSPx 2005
Pervasive Signal Processing
Conference and Expo

Oct 24 - 27, 2005 • Santa Clara Convention Center • Santa Clara, CA USA

KEYNOTE SPEAKER
"Broadband Wireless Opportunities and Challenges"
Dr. Andrew J. Viterbi
Pioneer in Wireless Communications,
Co-founder of QUALCOMM and creator of the Viterbi Algorithm

KEYNOTE SPEAKER
"Signal Processing Catches the Multicore Wave: Which Architecture is Right for Your Application?"
Dave Mothersole
Chief Technology Officer, Networking and Computing Systems Group and Director of Advanced Technology Development,
Freescale Semiconductor

KEYNOTE SPEAKER
"Mobile OFDMA for Triple Play Services"
Dr. Rajiv Laroia
CTO of QUALCOMM's OFDMA division (former CTO and founder of Flarion, acquired by QUALCOMM)

"Signal processing has become the technology driver for the entire electronics industry...because it is the basis of our mobile communications and multimedia future."
— Will Strauss, Industry Analyst, President, Forward Concepts

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KIC Group TECH BRIEFS
• **VIDEO COMPRESSION**

**MICROSOFT CORPORATION VC-1**

**DR. SRIDHAR SRINIVASAN, WINDOWS CORPORATION, DEVELOPMENT LEADER OF WINDOWS MEDIA CODECS GROUP**

- This tutorial is an introduction to the VC-1 bitstream format, and is intended for a diverse audience. First, we look at the Windows Media ecosystem, the relationship between the VC-1 format and its implementation WM9. We present an architectural overview of VC-1 and describe its various functional blocks. We also discuss standardization issues. In the next part of the tutorial, we consider aspects of implementation of the VC-1 decoder including profiles & levels, as well as computation issues. We examine blocks that may require optimization. We wind up this discussion with a look at the conformance requirement and post processing for visual quality improvement.

- In the third part, we look at an implementation of a VC-1 encoder. We list all the degrees of freedom provided by the bitstream and study their usage. We provide a guideline for implementers who must decide which features to support in a phased manner. We also discuss rate control issues, panic and special modes as well as optimization and pre processing.

- In the final part of the tutorial, we provide an overview of the steps involved in putting together a VC-1 enabled end-to-end system. Here, we briefly cover WMMA and WMM-DRM, together with transport issues and a look at Microsoft porting agreements, support offerings and roadmaps.

**H.264/MPEG-4 AVC CODER**

**DR. MARTA KARCZEWICZ, SENIOR RESEARCH MANAGER, NOKIA RESEARCH CENTER**

- **History of the development of the MPEG-4 AVC standard**
- Brief comparison of MPEG-4 AVC with previous standards.
- Detailed discussion of new Video Coding layer elements: context-adaptive variable-length coding (CAVLC) and context-adaptive binary arithmetic coding (CABAC), in loop deblocking filter, exact-match transform coupled with quantization matrix, directional, spatial domain intra prediction, motion compensation and prediction utilizing variable block sizes, multiple reference frames and quarter-sample accuracy. Costs and benefits of each tool will be considered - impact on coding efficiency versus impact on complexity.

- System integration of H.264/AVC codec.
- New standardization initiatives: Scalable Video Coder (SVC), Multi-View Video Coding and H.265.

**VIDEO COMPRESSION IN SURVEILLANCE: A CASE STUDY OF THE CITY OF LONDON**

**PETER FRY, DIRECTOR OF THE CCTV USER GROUP, UK**

**WIRELESS**

**WIMAX**

**MR. NAFTALI CHAYAT, CHIEF SCIENTIST, ALVARION**

The tutorial will cover the WIMAX and the underlying IEEE802.16 standard. The first part of the tutorial will focus on the WIMAX for the Fixed Wireless Access applications, while the second will cover the underlying principles of Mobile Broadband Access based on 802.16e standard.

- **Part 1**
  - Market background of WIMAX
  - Principles of OFDM and upstream OFDMA
  - Principles of 802.16 MAC
  - Support of Advanced Antenna Systems in 802.16

- **Part 2**
  - Mobile WIMAX - market background
  - OFDMA based physical layer
  - AAS and MIMO extensions
  - 802.16e MAC extensions for mobility
  - Summary

**UWB AND ZIGBEE**

**PATRICK KINNEY, KINNEY CONSULTING LLC, CHAIR, IEEE 802.15 TG4A, COVICE CHAIR, IEEE 802.15, CHAIR, ZIGBEE GATEWAY WG**

This tutorial will cover wireless technologies from the ZigBee Alliance and also Ultra Wideband (UWB) initiatives such as WiMedia, Wireless USB, and UWB Forum as well as the standards efforts behind these technologies.

- **Part 1 ZigBee Alliance**
  - Market background
  - Overview of Network layer
  - Overview of Application Support Layer
  - Description of the IEEE 802.15.4 PHY and MAC
  - Competing technologies such as 2-Wave, etc.
  - Summary

- **Part 2 UWB**
  - Principles of UWB
  - Regulatory environment of UWB
  - Market background of multimedia
  - Descriptions within multimedia UWB: WiMedia, Wireless USB, and the UWB Forum
  - Overview of IEEE 802.15.3a standards effort
  - Market background of ranging/location awareness
  - Overview of IEEE 802.15.4a standards effort

**ADVANCES IN WIRELESS LOCAL AREA NETWORKS - LAN AND MIMO**

**DR. BENNY BING, ASSOCIATE DIRECTOR OF THE GEORGIA TECH BROADBAND INSTITUTE, EDITOR IEEE WIRELESS COMMUNICATIONS MAGAZINE**

- **Topic 1**: Introduction to wireless LANs, including its evolution, standards and evolving technologies.
- **Topic 2**: Fundamentals of Wireless LAN Design and Deployment covers radio spectrum trends, physical layer transmission, MAC protocols, network topologies, security, switches, and deployment considerations (e.g., office, home, public hotspots/hotzones).
- **Topic 3**: 802.11 Wireless LAN Standards summarizes current 802.11 standards.
- **Topic 4**: Emerging 802.11 Standards discusses new 802.11 initiatives focusing on high-speed MIMO systems (802.11n), intelligent wireless systems (802.11k), wireless mesh networks (802.11s).

**MULTI-CORE PROCESSORS**

**BENCHMARKING MULTI-CORE PROCESSORS BASED ON PROCESSING THROUGHPUT**

**DR. WINTHROP (WIN) W. SMITH, ENGINEERING FELLOW RAYTHEON COMPANY, LEADER IN MULTI-CORE PROCESSOR CHIP & BOARD/BOX LEVEL**

Focused look on Multi-core Processors. From architecture to implementation to software development through 5 key lectures and sessions on Multi-Core Processors Chip and Board/Box Level. Sessions with the participation of:

- Analog Devices
- Codito Technologies
- Intel Itanium Group
- Intel Xeon
- Hewlett Packard
- GEDEE
- IBM Blue Gene Group
- IBM Cell Processor Group
- IBM Power Pc Group
- Philips Silicon Hive Processor
- IMEC

**SYNTHETIC APERTURE RADAR IMAGERY**

**CUTTING EDGE MULTI-DIMENSIONAL SAR IMAGE EXPLOITATION TOOLS FOR REMOTE SENSING, SURVEILLANCE AND TARGET DETECTION**

**DR. CHRIS OLIVER, CBE, LEADER IN SAR IMAGING**

These lectures are directed towards the fundamental physical principles that determine our ability to extract information from SAR imagery. Many of these fundamental principles can be found in ‘Understanding SAR Images’, by Oliver and Quegan, now republished by SciTech (ISBN 1-891121-31-6). However, the presentations contain considerable developments of these principles undertaken over recent years. The presentations are divided into 5 lectures addressing: SAR image formation, detection and correction (lecture 1); Information from SAR intensity (lectures 2 and 3); Information from polarimetric imagery (lectures 4 and 5). The lectures will start by examining the physical basis that underlies the information, introducing suitable models to represent the data, proposing algorithms for optimal information extraction, and discussing application examples.
**INTRODUCTION TO VIDEO COMPRESSION-SESSION 1 OF 2**

**MONDAY, OCT 24 • 1:00 PM – 2:30 PM**

Jeff Bier, Berkeley Design Technology, Inc., BDTI

Video compression algorithms ("codecs") manipulate video signals to dramatically reduce the storage and bandwidth required while maximizing perceived video quality. Understanding the operation of video codecs is essential for developers of embedded systems, processors, and tools targeting video applications. For example, understanding video codecs' processing and memory demands is key to processor selection and software optimization. In this presentation, we explore the operation and characteristics of video codecs. We explain basic video compression algorithms, including still-image compression, motion estimation, artifact reduction, and color conversion. We discuss the demands codecs make on processors and the consequences of these demands.

**PREPARING SOFTWARE FOR MULTI-CORE PROCESSORS**

**MONDAY, OCT 24 • 8:30 AM – 12:30 PM**

Lori Matassa, Intel Infrastructure Processor Division, Intel

This workshop is focused on the task of migrating software from a single processor to a multi-processor environment, particularly addressing customers migrating to dual-core processor architectures. The first half of the workshop will peel back the onion of the software stack and explain the implications for operating systems, libraries, drivers, and tools. Strategies for maximizing performance through multi-tasking, application partitioning and application threading are compared. The basics around parallel software are presented, including how to express parallelism to software tools, determine the correctness of code, and assess the resulting code performance. The second half of the workshop is targeted at software developers by providing a more detailed perspective on threading and scalability with respect to applications analysis, decomposition, measurement and relevant tools. Participants may elect to attend the first half or full day workshop.

**MODEL-BASED DESIGN FOR VIDEO SYSTEMS ON EMBEDDED DSPS**

**MONDAY, OCT 24 • 8:30 AM – 12:00 PM**

The MathWorks

Model-Based Design is a complete design flow that enables developers to use a single executable model of their entire system for algorithmic exploration; system design, simulation, and visualization; implementation with automatic code generation; testing, validation, and design verification.

In this workshop, we will apply Model-Based Design using Simulink® from The MathWorks to design, implement, and verify video applications on TI DSPs. Attendees will be exposed to all the steps of system design, including modeling, simulation, code generation, implementation on TI DSPs, and verification of the generated code in real time. Two video application examples — edge detection and video stabilization — will be used as the design examples.

We will then create models of the application in Simulink with the Video and Image Processing Blockset, simulate the model to validate algorithms, and convert the model to a fixed-point data type for embedded implementation. Using Real-Time Workshop and the Embedded Target for TI C6000 DSPs, C-code will be automatically generated for execution on a T1 C6416 DSK. The generated code will then be verified in real time, in the same environment using the Link for Code Composer Studio.

**STREAMLINING WAVEFORM PORTABILITY ACROSS FPGA ARCHITECTURES**

**MONDAY, OCT 24 • 8:30 AM – 12:00 PM**

Synplicity, Inc. (http://www.synplicity.com) has introduced their Digital Signal Processing development tool for Field Programmable Gate Arrays (FPGAs). The new tool, Synplicity® DSP, drastically simplifies algorithm development, area/speed performance, and portability for SDR applications. When used in conjunction with their Synplicity® IP Blockset, it provides the foundation needed for creating an FPGA-based Digital Down Converter (DDC). This tutorial will demonstrate the design of a Digital Down Converter algorithm generic to a Software Defined Radio. The implementation will show the ease of modeling using a DSP level blockset that is independent of any hardware implementation details. After modeling, the implementation will be simulated, analyzed, and then automatically implemented in an FPGA. We will then demonstrate the automatic re-targeting to a different FPGA, without any changes to the system model. The methodology and implementation in the Synplicity® DSP and Synplicity® IP Blockset tools, achieves that goal of waveform portability in the FPGA hardware implementation path. This approach is additionally portable to ASIC implementations.
In this presentation, we provide the background needed to select a processor for a consumer media product. We begin by exploring the types of processors used in these applications, including general-purpose CPUs, DSPs, media processors, and application-specific standard products. We characterize the strengths and weaknesses of each type of device, and evaluate leading processors in terms of performance, efficiency, development infrastructure, and vendor strategies. We present a logical, step-by-step processor-selection methodology, and highlight key trends in the rapidly changing processor landscape.
AEROSPACE AND RADAR
• High Performance FPGA Computing Platform for a Closed-Loop Flight Control Turbulence Detection System
• Heterogeneous Implementation of an Adaptive Bayesian Bayesian Radar
• Radar Processing Heterogeneous Future Technologies
• Wideband High Resolution ADC Technique Validated by Residual Error Analysis

ALGORITHM IMPLEMENTATION
• Efficient Methodology for Implementation of Matrix Inversion in Fixed-point Hardware
• An Efficient Implementation of Canonical Minimum Redundancy Prefix Code
• Biosignal Signal Solution of a General Purpose Hilbert Transformer Operating over more than Two Frequency DQnals
• Reconfigurable Matrix Multiplication For Reconfigurable Devices
• A Novel Method for Jitter Separation Based on Gaussian Mixture Model

ARCHITECTURES
• Challenges in PowerPC40-FS Soft Core Development: Timing Perspective
• Using Multiple Custom Instruction Configurations to Accelerate Computation of Algorithms
• Cache Based Adelante DSP for Application Driven SOC Evolution
• A Hardware Performance Analysis Framework for Architectural Exploration of DSP Systems
• Optimized Pipelined Time Shared Real Time Machine (OTSRM)
• Simulation Analysis of a Very Long Instruction Word Processor under Globally Asynchronous and Locally Synchronous Multi-Process Processor with Improved Efficiency
• Dynamically Reconfigurable Hardware Design for Low Latency Time
• VLSI Architecture for Video Compression Using HybridTransform
• Alternatives in New Controller Designs: SoC, SIP or Distributed Processing
• The Emergence of ASIC Disruptive Technology In - Standard Metal Out: Standard Cell
• Fast Track Third Party IP Core Integration - An Efficient Two Pass IP-Based ASIC Design and Verification Methodology
• The StarCore SC400 as a Mobile Application Processor Accelerator
• Design of Application-Specific Instruction-Set Processors for Multi-Media, using a Retargetable Compilation Flow
• Industry Trends and Challenges in Providing Small Farm Factor (SFF) HHD Technology to the CE Marketplace
• Bringing Automation to the Verification of SoC-Based Designs
• The Next-Generation Packet-Based Multi-Processor DSP: Architectural Considerations for Multi-Channel High Speed Data Acquisition in Sensor Processing Systems

AUDIO
• An Efficient Asynchronous Sampling-Rate Conversion Algorithm for Multi-Channel Audio Applications
• Designing and Debugging Efficient, Real-Time Audio DSP Systems in a Graphical Programming Environment
• An Audio Signal Processing System for Wired and Wireless Headsets
• Voyager: Ultra Low Power Reconfigurable DSP Platform for Personal Audio Systems
• Optimization of Vorbis I Decoder on TMS320C66x Platform
• Psychoacoustic model and audio compression
• A Development of a Vocal Suppressor with .NET Platform

AUTOMOTIVE
• Systems Software Requirements for In-Car Digital Entertainment
• When Cars Can See: How Automotive Vision Will Roll Out
• 1394-Automotive – TTP Gateway for In-vehicle Applications
• Hands Free Telephone - A Framework Based Approach
• Accelerating Automotive Video-Based Active Safety System Development with Model-Based Design
• The Digital Car - Are we there, yet?
• How FGAs Enable Automotive Systems
• Intelligent Road Sign Detection for Vehicle Video Processing
• Simulation Analysis of Re-engineered Legacy Engine Management System
• Assisted Lane Maneuvering System using Computer Vision

BIOMEDICAL
• Effects of Detection System on Surface Detected Motor Unit Action Potentials: A Simulation Study
• Precise Segmentation of Glazing of the Neuron Sterm Cells in Time Lapse Image Sequences
• Cancer Cell Recognition by Fuzzy Logic in Medical Images
• Classification of Malignant Signal Patterns using an Artificial Neural Network on a Multi-function Myoelectric Controller
• QT Interval Monitoring in ECG Signal and Syndrome of Sudden Death by using Kohonen Networks
• Medical Images Adaptive Compression for Transmission and Archiving Application to MRI Modality
• Positron Emission Tomography (PET)

BIOMETRICS
• Using Software-Configurable Processors in Biometric Applications
• A Robust Fingerprint Recognition Scheme
• Student Class Attendance Record Using Fingerprint Identification
• Fingerprint Image Enhancement using Composite Method
• Fingerprint Image Enhancement using Morphological Transform
• Face Recognition using Eigen Fonces Method

BROADBAND AND DATA COMMUNICATIONS
• Fiber Optic Microcellular Network
• Implementing a FPGA-Based Broadband Modern Using Model-Based Design
• Design of PGS Interface using Network Processor

CONSUMER ELECTRONICS
• 16 Bit Chassis and ISM Band Radio Application in Home Access Control
• Open Architecture Settop Box Platform
• Development of a real-time system to detect Audio Smoke Alarm
• Secure, Low-Cost On-Chip Firmware Storage for Embedded Signal Processing Systems
• An Effective Dynamic Handoff Support for Mobile Media Network
• Mobile Navigation Movie Player: A Navigation tool based on GPS and Streaming Multimedia Player

DIGITAL FILTERS
• Computationally Efficient Architecture for the Design of QMF Banks with CSD Coefficients
• Structural Simplicity of Multiprocessor Digital Filters
• Generation and Enumeration of Structures of IR Digital Filters
• Design of Multistage Filters Using DIOs
• Implementation of Digital Filters using FPGA

DIGITAL RADIO
• Optimisation of a Scalar Sampling DRF in an FPGA
• Flexible Architectures for Wideband SDR Channelisation
• Spectral Efficient Technologies in 3G for Packet Access
• Design Optimization of a DSSS Receiver Using Hardware Co-Simulation
• The Performance of the Modified Saturation Routing Algorithm in a Tactical Communication Network
• Software Defined Radio - Signal Processing Subsystems
• Development, Code Generation and Systems Integration
• Building Secure SCA-enabled SDR Hardware and Software

EMBEDDED SOFTWARE, SOFTWARE ARCHITECTURE AND SOFTWARE TOOLS
• A Hybrid Real-time, Secure, Operating Environment Supporting Windows and Linux
• Multi-lingual Compact Fonts for Digital Displays
• Power Efficiency for Real-time Embedded Systems
• How to Optimize Software Effectively in DSP Embedded Systems
• Emerging Web Technologies Needs - XML Based Rich Clients
• Coping with Algorithm Modifications During the Design Process
• A C Model for UMA3.x Architecture Evaluation
• Tool-Flow for An Automated Compilation of SIMULINK and Real-Time Workshop Applications onto Heterogeneous Platforms
• Linux as an Embedded Operating System and Development Environment
• Implementing a Multi-Threading Scheduler in a Real-Time Operating System for Digital Signal Processors
• Transaction-based Debug of Communication-centric Embedded Platforms
• Understanding DSP Synthesis
• Metrics-based Behavioral Design: A Methodology for Quickly Realizing High Quality Hardware for Signal Processing Applications
• Graph Theoretical Modelling and VLSI Design Framework for Entropy Based Signal to Memory Box

FOR [RF Engines], this is probably our favorite show of the year. It's well focused, in a good location and yields a good volume of sales leads. The companion conference also fits our interests really well. Although only in its second year, it feels like we have a great future and we look forward to next year.

— John Liington, CEO / CTO, RF Enginies Ltd.
PAPERS

Papers will be added. Be sure to visit www.gspx.com and check back often for updates.

MODELING AND SIMULATION
• Design and Verification of Communications Systems using Model Based Design
• Fast Bit-Accurate C++ Datatypes For Functional System Verification and Synthesis
• Instruction Set Level and System Level Co-Verification
• A Framework for Fast Simulation of DSP Algorithms on Multiprocessors
• Building a Complex SystemIC System by Reusing Legacy C++ Models
• Consolidated Modeling Approaches at the System Level Support Flexible Implementation Paths
• Design and Implementation of Embedded Motor Controllers
• Modeling and Analysis of LiFeO2 Optical Modulator with Superconducting Electrodes

MULTI-CORE/MULTIPROCESSING
• Common Programming Models with a Dual-Core Processor
• Using a Dual-core Processor in Power-Sensitive Applications
• Acceleration of Signal Processing Applications Using Parallel FPGA-Based Processing Boards
• Code Partitioning – Optimizing an Asymmetric Multi-core System
• A Framework for the Automatic Generation of Audio Processing Applications on a Dual-GPU System
• Optimizing Inter-processor Communication on Freescale 1300-30 Multi-core Platform
• A Multi-core Structure for In-Car Digital Entertainment
• A Multiple Core Distributed MPEG4 High Resolution Decoding Solution on Freescale 1300-30 Innovative Convergence™ Platform
• Programmability Solution for Embedded Applications on Multi-core and Multi-processor Architectures
• Large FPGAs on a Cell Processor
• Designing and Implementing a Solution for the Viterbi Codec on the Xilinx Virtex-5X ML503 Platform
• A new Single Instruction Multiple Data (SIMD) Processor
• Compiler-Synchronized Multithreaded System Based Programmable Device
• HP presents dual core performance characterization using results from work with commonly-used ISV codes, and discusses implications for optimizations and system configurations.
• An H.264 compatible video encoding algorithm on a CellProcessor
• Audiosignal Sensor Processing Applications to Run on Multi-core Processors
• Automation in Single Chip Parallel Programming - The "Cascade" Language
• Blue Gene/L Packaging
• OpenBayBoard Engine support for privacy, security, and digital rights management applications
• Code Partitioning – Optimizing an Asymmetric Multi-core System
• Construction of a Parallel MPEG4 Video Decoder on a Multi-core Architecture for Broadcast Applications
• Delivering Scalable Software on BlueGene/L
• Enabling Software-Programmable Multi-Core Systems-on-Chip for Consumer Applications
• Exploiting Parallelism, While Managing Complexity using Silicon-Hive Programming Tools
• Gedeo for Multi-processor Systems - Implications of Multi-core Processing
• Gedeo Language Features for FPGA and Multicore Programing
• H.264 Scalizable Video Coding Array plans using multi-core systems and advanced graphics processing units
• Implementing Motion Control on Multiple Processor Systems
• Life Sciences on Blue Gene/L
• Littleplan’s Supercomputing Have Arrived - Blue Gene/L Overview
• Multi-core and hyperthreading resource management for clusters based on work done in HP Advanced Development by an internal lab scale
• Multi-core futures for HP platforms - roadmap for the three processors in next year
• Multi-Core Processing Improvement Analysis for RADAR STAP Processing
• Multi-Core Architecture for Digital Video Reception and Video Processing
• Ranged Embedded Clusters for DOD programs with 10G Myrinet switch fabric and FreeScale
• Server Capabilities of Intel’s next generation Itanium®(r) Server Processor
• Silicon Hive’s Scalable and Modular Architecture Template for High-Performance Multi-Core Systems
• Technical Details of Intel’s next generation Itanium(r) Server Processor
• Teramin Rendering Engine (TRE). Cell processors Optimized Real-time Ray-caster

NETWORKING
• Access to Ethernet Gateways Pave the Way to IP
• Enhancement and Performance Analysis of Industrial Ethernet
• FPGA Implementation of High-speed Symmetric Crossbar Switchers for VLAN Switches
• A Fuzzy Logic Based Approach for QoS Routing in Computer Network

POWER MANAGEMENT
• Topics on Power Management in Cellular Systems
• Industry Trends in Power Management Technology for the CE Marketplace
• Obtention of a Power Management Scheme for an Embedded System through Simulation
• Power Architecture for CompactPCI Platforms

PROGRAMMABLE AND PROGRAMMING DSP
• Philips Semiconductors Adapte VD32040 Architecture. An Embedded Vector Processor for Low Power DSP Applications
• LSIs ZSP3560C Processor: A Media Processor for Real-time DSP Applications
• Critical Decoding System Designers on Performance, Price, Power, Peripherals
• Enabling Use of Dynamic Storage Allocation in Real-Time Embedded DSP Applications
• Analysis of Loan of Selectable Mode Codec and Its Impact on Instruction Level Parallelism
• High-Performance DSP Programming with Embedded C
• Parting open-source Algorithms to Advanced Digital-signal processors
• Accelerating Compute Intensive Functions Using C and Software-Configurable Processors
• Optimization of MPEG/2 AAC Decoder on TMS320C6x Platform
• CD++ Loop Transformations for Hardware Synthesis
• Optimum Register and Functional Unit Assignment for VLW DSPs: A Case Study
• Programming the ITU-TSC CRC32 Algorithm in High-speed PowerPC AltiVec Assembly Language
• Optimizing the GNU C Compiler for the TMS320C60x DSP
• A Secure, Field Upgradable Operating System Architecture for Blackfin Microprocessors

SPEECH PROCESSING AND RECOGNITION
• Output Based Speech Quality Assessment in Mobile Communications Using Hidden Markov Model
• Automatic Gain Control for Speech and Audio Signals
• Clustering Techniques at the Subvector Level for Discrete Mixture HMM (DMHMM) Acoustic Models
• Microphone Array Geometry for Interference Suppression with Robustness Against Inaccuracies in the Far-Field Assumption
• Improving SNR of Speech Signal by Spectral Subtraction method using Matlab and VHDL
• A Pitch Detection-based Doubletalk Detector
• Discrete Words Speech Recognition Using Self-adaptive Hidden Markov Model (HMM)
• Implementation of SGPC Based Isolated Word Recognition System
• Isolated Word Recognition using Dynamic Time Warping
• Effect of Speech Rate on Speech Recognition Accuracy

VIDEO BROADCASTING AND RECODING
• Implementing a Single-Core DVB-H Player on a StarCore SC4200 Processor
• An Efficient Motion-Adaption De-interlacing Technique on VLW DSP
• Architecture
• Implementation of Motion Estimation Algorithms on Dynamically Reconfigurable Processor
• RapidIO in Video Infrastructure Systems

VIDEO COMPRESSION AND PROCESSING
• Software and Hardware Solution for Software and Hardware Solution for H.264 Video Decoder on HDTV Applications
• Instruction and Data Cache Optimizations for MPEG4 Decoding on Freescale 1300-30 Innovative Convergence™ Platform
• H.264 Video Encoding Algorithm on a Cell Processor
• SVNC - Scalable Video Engine for the High Definition TV Market
• Media Processor Architectures for Mobile DVB-H Terminals
• Implementation of H.264 Encoding Algorithms on a Software-Configurable Processor
• A Low Power Soft Core for Multi-standard Video Applications
• Low-Cost Solutions for Video Compression Systems
• Scalable FPGA Design for MPEG-4 Codec Applications
• Implementation of MPEG-4 Encoder on Sandblaster

VoIP
• Enabling Media Services in a VoIP Network
• Open Standards Solutions in the VoIP Communications Equipment Market
• Latency and QoS Management for Wireless VoIP
• Exploiting Parallelism, While Managing Complexity using Silicon-Hive Programming Tools
• HP Scalable Visualization Array plans using multi-core processors
• Gedae Language Features for FPGA and Multicore Programing
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• Technical Details of Intel’s next generation Itanium(r) Server Processor
• Teramin Rendering Engine (TRE). Cell processors Optimized Real-time Ray-caster
• Implementation of MPEG-4 Encoder on Sandblaster
• Realtime Optimization Techniques for Processor Based H.264 Intra Frame Compression
• Exploding Threat-level Parallelism in H.264
• Implementation of Video Codes using MIMD Processors
• Efficient Implementation of Video Encoder on Symmetric Multicore Processors
• A Dynamically Reconfigurable Stream Processor for Video Processing: Object-Oriented Approach using MPEG-4

WIRELESS COMMUNICATIONS AND TELEPHONY
• Developing 80G-16-2004 SDR Using a Software-Configurable Processor
• Beamforming Techniques for MIMO-OFDM Systems
• Analyzing the BER in the 3GPP2 and 3GPP Context
• An Improved Algorithm to Minimize Clock Offset Effect for 4G OFDM System
• Implementation of UEsynchronization Unit for 4G OFDM System
• GSM Baseband Optimization on a Parallel Processing Architecture
• A Channel Assignment Scheme for Wideband Systems
• Ultra Wideband (UWB) - Innovative Technology
• Channel Estimation using Kalman Filter for UWB Communications System
• On an OFDM-UWB System with Two-Adaptive Linear LMS Equalization
• Performance Evaluation of Multiband Orthogonal Frequency Division Multiplexing
• Full Rate FPGA-based Synchronization Circuit For Multi-band OFDM UWB Receiver
• VLSI Implementation of High Speed FFT Processor for UWB Multi-band OFDM
• A Sub-band Based Approach to Space – Time Adaptive Processing for UWB Multi-Access Systems
• FPGA based WIMAX System Design
• SW Implementation of High Performance 802.16 on a TigerSharc Processor
• Using Signal Processing Algorithms and RF Behavioral Models to Optimize Wireless Communication Designs
• Performance Analysis of Equalization Schemes for 802.11b Networks
• IP Strategies in Today’s Wireless Technology Revolution
• DSP Implementation of Adaptive Channel Equalizer to Overcome Intersymbol Interference in a Digital Cellular Communication
• Enhancing Data Efficiency in IEEE 802.11a using Equalization
• A Study on the Implementation of Authentication techniques for the CDMA Flight Termination System
• Simulation of Adaptive Modulation
• High Rate Turbo Equalization Based on LDGM Codes
• A Novel Channel Estimation Method for OFDM Mobile Communication Systems Based on Pilot Signals and Divided Wavelet Transform
• Air Interface Technologies for Evolved UMTS
• Adaptive Channel Estimation Techniques for OFDM Systems in Doppler Channels
• COHC-Based RLS Algorithm Via Symmetric Array Mechanism
• Enabling New Technology Adoption into Portable Embedded Systems
• UMTS and HSDPA Implementation on the StarCore SC1400 Processor
• Satellite IF
• Multi-chip Remote File System
• Performance and Quality of Service Management in GPRS Network
• Design of CDMA Matched Filter Chip using VHDL and Implementation in Vertex Device using Reconfigurable Architecture for CDMA

PERSIAN Vehicular Signal Processing Conference and Expo
Oct 24 – 27, 2005 • Santa Clara Convention Center • Santa Clara, CA USA
NEW PRODUCT FORUM  TUESDAY, OCTOBER 25, 2005 – 1:00 PM

Do You Have a New Hardware or Software Product that Will Be Introduced at GSPx?
If so, we want to hear from you!

Your audience will be expo and conference attendees plus trade and business press editors.

Submissions should only be for new hardware and software products, not previously announced prior to GSPx 2005, in the areas of signal processing, DSPs, embedded applications, and EDA tools for developing signal-processing chips or subsystems.

The deadline for New Product Forum submissions is SEPTEMBER 26, 2005.

Please send your submissions, not to exceed 400 words, to Jim Lipman (ednjim@earthlink.net) and Will Strauss (wis@fwdconcepts.com) to be eligible for consideration. You may include no more than two graphics with your descriptions. We will honor embargos up to the October 25 date. Please include a contact person name, phone number and email with your submission.

We look forward to receiving your entries for the GSPx 2005 New Product Forum and hope to see you at the show!

For information on GSPx, go to www.gspx.com.

Sincerely,

Will Strauss
President, Forward Concepts

Jim Lipman
Vice President, Cain Communications
### GSPX 2005 EVENT REGISTRATION FORM

#### STEP 1: NAME & ADDRESS

<table>
<thead>
<tr>
<th>field</th>
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<tbody>
<tr>
<td>Name</td>
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<td>State/Prov.</td>
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#### STEP 2: WORKSHOP SELECTION

<table>
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<th>Selection</th>
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<tr>
<td>8:30 am - Noon</td>
<td>WRITE MORNING WORKSHOP SELECTION HERE</td>
</tr>
<tr>
<td>1:30 pm – 4:30pm</td>
<td>WRITE AFTERNOON WORKSHOP SELECTION HERE</td>
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#### STEP 3: FEES AND PAYMENT / CIRCLE YOUR CHOICES

<table>
<thead>
<tr>
<th>Promotions Code</th>
<th>INDUSTRY GSPxRI</th>
<th>ACADEMIA GSPxRA</th>
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<tr>
<td>GSPx Technical Superpass</td>
<td>$1295</td>
<td>$995</td>
</tr>
<tr>
<td>GSPx Technical Conference</td>
<td>$950</td>
<td>$650</td>
</tr>
<tr>
<td>GSPx Expo Only – No Charge</td>
<td>Includes access to the Exhibit Hall.</td>
<td></td>
</tr>
<tr>
<td>Additional CD-ROM Proceedings (On-site pick-up only)</td>
<td>$150</td>
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**GSPx Technical Superpass** includes access to all Tutorials, Workshops, Conference Tracks, Technology Panels, proceedings on CD, admission to Keynote Presentations, New Product Forum and the Exhibit Hall.

**GSPx Conference Tracks** includes access to all paper Presentations, Technology Panels, proceedings on CD, admission to Keynote Presentations, New Product Forum and the Exhibit Hall.

**GSPx Expo Only – No Charge** Includes access to the Exhibit Hall.

#### STEP 4: METHOD OF PAYMENT

<table>
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<tr>
<td>AMEX</td>
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</table>

Credit Card # Expiration Date

Print Name (as it appears on card)

Signature

**Payment Policies:** Full payment must be made at the time of registration. You may register and submit payment to the event online or by Fax at +1 617-243-9797 using a Visa, Master Card or AMEX.

Cancellations & Substitution Policies: You may cancel in writing to Global Technology Conferences. Cancellations before August 30, 2005 will receive a refund. You may fax your cancellation request to +1 617-243-9797. There is no cancellation for accepted authors presenting at the conference.

Recording devices and cameras are not allowed at the Conference or Expo. Children under 18 are not admitted to the show.

**Registration Fax +1 617-243-9797**

To register: Please fill out the Event Registration Form and fax it to +1 617-243-9797. If paying by check, please fill out the Event Registration Form and mail it with a check drawn on a US bank to Global Technology Conferences, 1320 Centre Street, Suite 200, Newton Ctr., MA 02459 USA. For more information, contact info@gspx.com (or phone 1-617-243-9777).

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