CHAPTER MEETINGS

SCV-Nano - 5/29 | **Intellectual Property Strategy For Entrepreneurs, Technologists & Business Leaders** – planning, patents ... [more]

SCV-Rel - 5/30 | **Designed Experiments and Reliability** - redefine the problem to simplify and optimize ... [more]

SF-PES - 5/30 | **The Renaissance of Nuclear Power** - annual banquet plus two speakers ... [more]

SF-EMB - 5/30 | **Physiological MR Imaging and Spectroscopy of Brain Tumors** - malignant progression of tumors ... [more]

SCV-CS - 6/2 | **Multicore: the New Face of Computing -- Promises and Challenges** - where it stands, issues to be addressed ... [more]

SCV-PACE - 6/4 | **Who Wants to be a Start-Up Star?** - Silicon Valley, venture capital firms, and knowing how to be the Talent ... [more]

SCV-LEOS - 6/5 | **Progress in Reliable High-Power Diode Lasers** - near infrared diode lasers and applications ... [more]

Careers-GOLD - 6/9 | **Tri-Section GOLD Networking Event** - Grads Of the Last Decade: growing your career, free breakfast ... [more]

SCV-Mag - 6/12 | **Long Data Sectors, Capacity Growth and Data Integrity in HDD's** - coding solutions to resolve the bottleneck ... [more]

SCV-CPMT - 6/13 | **uPILR MicroContacts: A Next-Generation Chip-Scale Packaging Solution** - for density and routing efficiency ... [more]

SCV-CE - 6/19 | **Biometrics: Finger Print Sensor Technology** - cost effective security solution ... [more]

SCV-Nano - 6/19 | **Polymer Nanocomposites: Fabrication, Characterization and Application** - polymer resins filled with particles ... [more]

SCV-EMB - 6/20 | **Bionic Technology for Mobility Assistance** - active orthotics, bionics, bio-robotics, and exoskeletons ... [more]

OEB-IAS - 6/21 | **So what's Wrong with your Data Center or UPS Designs?** - common deficiencies and solutions ... [more]

SCV-PSE - 6/26 | **Telecomm Topics – FAQs (and Answers)** - safety issues with power-over-ethernet, TNV ... [more]

Monterey - 6/28 | **Exploring the Ocean Using Autonomous Underwater Vehicles** - architecture, various sensors, results ... [more]

SCV-SSC - 6/28 | **First Time, Every Time: Practical Advice for Phase-Locked Loop Design Success** - in a CMOS world ... [more]

SF-GOLD - 7/15 | **IEEE GOLD Networking Event & Hike at Land's End** - explore the beauty of the SF coast with fellow grads ... [more]

SCV-CE - 7/24 | **DisplaySearch Projections for HDTV** - new technology development, shipments, forecasts ... [more]

SCV-CE - 8/28 | **WirelessHD: High Bandwidth for Home Entertainment** - what's being planned for your home ... [more]

SCV-Mag - 9/15 | **State-of-the-art Ferrite Materials for Fundamental Research, Nano-science, and High-Frequency Applications** - [more]

Upcoming Conferences

June 4-8: **44th Design Automation Conference** (DAC07) - San Diego [more]

June 7-8: **Frontiers in Biomedical Devices 2007** - Irvine, CA [more]

Jun 25-27: **POFWORLD WEST 2007 -- Plastic Optical Fiber Conference** - Santa Clara Conv Center [more]

Aug 7-9: **Flash Memory Summit 2007** - Santa Clara Marriott, Santa Clara [more]

Sept 5-7: **Energy Nanotechnology Int'l Conference** - Santa Clara University [more]

Santa Clara University Graduate School of Engineering
Summer Open University Classes [more]

Tutorials from local IEEE Chapters

Multicore -- the New Face of Computing: Promises and Challenges - Saturday, June 2 [more]

Broadband Circuit Analysis/Design in CMOS - Saturday, June 16 [more]

Professional Skills Courses

- **Managing Time and Multiple Priorities**
- **Budgeting Essentials**
- **Management Essentials**
- **Clear Business, Technical, and E-mail Writing**
- **Getting Things Done Across Organizational Borders**
- **Managing Time and Multiple Priorities** [more]

Technical Skills Courses (sponsored by SCV Section)

Analog CMOS Integrated Circuit Design
Design of Radio Frequency Integrated Circuits
Digital VLSI Design with Verilog
Statistical Process Control (SPC)
Signal Integrity (SI) and Noise Issues in Nanometer VLSI/SoC Designs
Reliability & Failure Analysis of Advanced Semiconductor Devices & Products
Advanced Semiconductor Technology & Fabrication
Advanced Script Writing in TcL [more]

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IEEE GRID

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for news for technologists, managers and professors, the editorial objectives of IEEE **GRID** are to inform readers of newsworthy IEEE activities sponsored by local IEEE units (Chapters, Affinity Groups) taking place in and around the Bay Area; to publicize locally sponsored conferences and seminars; to publish paid advertising for conferences, workshops, symposia and classes coming to the Bay Area; and advertise services provided by local firms and entrepreneurs.

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From the editor . . .

As the SF Bay Area extends its technological reach into additional related fields, the IEEE locally is also growing – developing new Chapters to serve the needs of our Members and other professionals. I'd like to highlight a few such expansions that are going on right now:

First, the Santa Clara Valley Section is starting a new chapter in Robotics and Automation. Being headed up by Ed Katz, at Carnegie-Mellon University West, it should have its first meeting in September or October. Ed invites you to give him some help, if this is your field (or your interest): e.p.katz@ieee.org

Another field being addressed by the SCV Section is Power Electronics – critical for power conditioning in computers, vehicles, motors, solar energy conversion, and other fields. Ari Shrager at ETM Inc in Fremont will be the acting chair as this chapter kicks off evening meetings in the fall. Contact Ari if you can help him get things going: ashrager@etm-inc.com

The intersection between biology and technology gets reported at monthly meetings of the Engineering in Medicine and Biology Chapter. Until recently there has only been the SCV Chapter, meeting at Stanford. Now the SF Section has formed a new EMB Chapter that will meet in San Francisco and potentially in Berkeley. To assist Bob Giebele as he develops the program, email him at: bgif251@yahoo.com

The Bay Area is again in a growth mode for the application of technology to society's problems; we should be proud to be a part of this effort!

Paul Wesling, editor

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

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The Only Trade Show Dedicated To Plastic Optical Fiber Technology & Applications

POFWORLD WEST 2007

Tutorials: June 25 | Conference: June 26-27, 2007

Santa Clara Convention Center | Santa Clara, CA

Attend POFWorld West in Silicon Valley! One of the main focal points of POFWORLD WEST 2007 will be "POF in Video and Surveillance Applications" in addition to the latest in POF technology for both data and non-data applications. POF is being promoted in Europe by the major telephone companies as a method to guarantee the "Quality of service" of IPTV service. Set-top boxes have been developed with POF interfaces to connect over POF fiber to TV sets. For in-house wiring using IEEE-1394, media converters have been recently introduced to convert coax to POF.

Exhibits – Multi-attendee discounts.

Organized by

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Information Gatekeepers, Inc.

Morning Tutorial:

POF Markets, Technology, Standards and Applications
Dr. Paul Polishuk, President, IGI Consulting, Inc.

Sessions:

POF Data Applications (POF in Security and Surveillance; Applications in Aircraft; Ultra-short Reach Optics; Optical Fiber Sheets; Board-level Optical Interconnects)

POF Non-Data Applications (Hybrid Solar Lighting System; Industrial Process Controls; Environmental Monitoring; Lighting and Signage; LED Lighting)

POF Technology (Perfluorinated Fibers; High-temperature Materials; IPTV; Video Surveillance)

New Opportunities for POF (10 Gigatbit Data; 100G Status; 40Gbps Links; Storage Area Networks; New Products)

Save $100 through May 25, 2007!

For more information and to register, visit

www.POFWorld.com CLICK!

IEEE Professional Skills Courses

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Managing Time & Multiple Priorities

- Date/Time: Tues, June 12, 9:00 AM – 1:00 PM
- Location: Synopsys, Sunnyvale
- Fee: $275 for IEEE Members; $325 non-members

Budgeting Essentials

- Date/Time: Wed, June 13, 8:30 AM – 12:30 PM
- Location: VeriSign, Mountain View
- Fee: $275 for IEEE Members; $325 non-members

Management Essentials *new!*

- Date: Thurs-Fri, June 14-15, 8:30 AM – 4:30 PM
- Location: Trimble Navigation, Sunnyvale
- Fee: $600 for IEEE Members; $675 non-members

Clear Business, Technical, and E-mail Writing

- Date/Time: Thurs, June 14, 8:30 AM – 4:30 PM
- Location: TIBCO Software, Palo Alto
- Fee: $400 for IEEE Members; $475 non-members

Getting Things Done Across Organizational Borders

- Date/Time: Thurs, July 12, 8:30 AM – 4:30 PM
- Location: TIBCO Software, Palo Alto
- Fee: $375 for IEEE Members; $450 non-members

High-Impact Communication

- Date/Time: Tuesday, Aug 21, 8:30AM – 4:30PM
- Location: Tibco, Palo Alto
  Fee: $375 for IEEE Members; $450 non-members

Improve your skills – register for one of these classes, or for others coming up this summer. Bring a team!

For complete course information, schedule, and registration form, see our website:

www.EffectiveTraining.com

June 7-8, 2007 Irvine, California

2nd Frontiers in Biomedical Devices Conference

The ASME Nanotechnology Institute, in cooperation with the IEEE's Engineering in Medicine and Biology Society, is pleased to announce the 2nd Frontiers in Biomedical Devices conference, to be held June 7-8 in Irvine. Leading authorities in the commercial and academic arenas will focus their expertise in nine technical tracks plus posters:

- Imaging & Monitoring the Environment
- Simulation & Modeling
- Device Testing
- Bio-Sensors & Diagnostics
- Device Design & Development
- Therapeutic Devices
- Next Generation Device Technology
- Clinical & Regulatory
- Posters / Student Posters

Our program will be co-chaired by **Abe Lee, Ph.D.** of the University of California's Henry Samueli School of Engineering's Biomedical Engineering Department, and co-chaired by **Walt Baxter, Ph.D.** of Medtronic Cardiac Rhythm Management.

WHO SHOULD ATTEND

Medical device engineers, research scientists, government & academic personnel, and those involved in medical device research, discovery, clinical evaluation and delivery of medical devices are encouraged to attend.

The conference also includes an evening reception/ exhibition/poster session/panel session (with OCTANe) on June 7th at the hotel. Posters will be presented and displayed during the conference.

The **Hyatt Regency Irvine hotel** is conveniently located near the John Wayne Airport.

For more information and to register,

visit: **www.asmeconferences.org/biomed07**

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Contact Brandy Smith at smithb@asme.org
or 917-596-0306

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Summer Courses with labs

Analog CMOS Integrated Circuit Design

12 week course, M/W 6:00PM-9:00PM (Starts **May 30**)
A detailed review of principles, concepts, and design methods used in the design of current state-of-the-art analog circuits. HSPICE simulations and labs are used extensively to augment the text/lecture material.

Design of Radio Frequency Integrated Circuits

12 week course, T/TH 6:00PM-9:00PM (Starts: **June 12**)
A balance of communications, physics and IC design. Includs high-speed amplifiers, LNA, Mixer, VCO, PA, PLL and other RF blocks.

Digital VLSI Design with Verilog

12 week course, T/Th 6:00PM-9:00PM (Starts **June 19**)
Design of digital ICs using the Verilog digital design language. Using a balanced mixture of lecture and lab, the students are introduced to language constructs in a progressively more complex project environment.

Discount of $40 for IEEE Members on 12-week courses.

Upcoming 1- and 2-day Seminars:

June 12: **Statistical Process Control (SPC) - Principles and Application**

June 14: **Signal Integrity (SI) and Noise Issues in Nanometer VLSI/SoC Designs**

June 19: **Advanced Script Writing in TcL**

June 21: **Reliability & Failure Analysis of Advanced Semiconductor Devices & Products**

June 28-29: **Advanced Semiconductor Technology & Fabrication**

Discount of $30 for IEEE Members on Seminars.

Get more information: CLICK!

www.svtii.com/SVTI-calendar.htm

Review all SVTI offerings: **www.svti.org**

44th Design Automation Conference

San Diego June 4-8, 2007

Technical Theme:
Automotive Electronics

Soon, thousands of us will converge in San Diego to attend the Design Automation Conference, the largest and most prestigious annual event focused on the design of electronic circuits and systems. DAC is the premier Electronic Design Automation (EDA) and silicon solution event. DAC features over 50 technical sessions covering the latest in design methodologies and EDA tool developments and an Exhibition and Demo Suite area with over 210 of the leading EDA, silicon and IP providers.

The DAC technical program is made up of 14 tutorials, 7 workshops, 17 DAC Pavilion presentations and 62 technical sessions divided into 11 tracks: Business; System-Level and Embedded Systems Design; MEGa; Low Power and Thermal; Analog and Circuit; Interconnect, Reliability and DFM; Verification and Test; Synthesis and FPGA; Physical Design; Beyond the Die; and New and Emerging Technologies.

Business Track: (all-day Tuesday)

Innovation or Extinction - the choice is yours! The business track begins with a morning keynote, and continues with an all-day management seminar presented by a group of luminaries: Geoffrey Moore, Raul Camposano and Jim Smith.

Keynote Speakers:

Designing a New Automotive DNA
Lawrence D. Burns, VP-R&D, General Motors
Perspective of the Future Semiconductor Industry: Challenges and Solutions
Oh-hyun Kwon, President, System LSI Division, Samsung
Design without Borders – ATribute to the Legacy of A. Richard Newton ***Prof. Jan M. Rabaey,*** Director Gigascale Systems Research Center, UC-Berkeley

Colocated and Adjunct Events:

* Design Automation Summer School
* IWLS
* MSE
* EDA Consortium Executive Reception
* EDA Consortium Productivity Impact Luncheon
* IEEE CEDA Distinguished Speaker
* SIGDA Ph.D. Forum

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Special Sessions:

• 1000-core Chips • Function Verification of ESL • Synthetic Biology • Trusted Hardware • Silicon Measurement • Virtual Automotive • Future Interconnect • WACI

Theme Day:

This year's DAC Theme Day, on Wednesday July 26, will focus on Automotive Electronics. The modern car can now truly be described as a "networked computing platform," and the theme will highlight this issue in the context of electronic design automation.

44th DAC Workshops & Tutorials (Sunday and Monday)

- **4th UML for SoC Design Workshop**
- **Low Power Coalition Workshop: Standards for Low Power Design Intent**
- **Design and Verification of Low Power ICs**
- **Hardware Dependent Software (HDS)**
- **Intro to Chips/EDA for a Non-Technical Audience**
- **Workshop for Women in Design Automation: Managing Your Career**
- **3rd Integrated Design Systems Workshop**
- **Anatomy of Variability and Making of "Variation Tolerance" Vaccine in Nanometer Technologies**
- **System Design for Multimedia Applications**
- **Standard Cell Library and Hard IP Design**

Substantial discount for IEEE and ACM members, students

"Free Monday" exhibits pass

Access the Advance Program on the website:

www.DAC.com

Flash Memory SUMMIT

2nd Annual Flash Memory Summit
August 7-9, 2007
Santa Clara Marriott
Santa Clara, CA

Learn how to make your products
Rugged, Low-Power, Fast and Small
at the only conference dedicated to flash memory!

Attend this year's Flash Memory Summit for the latest practical information on flash memory and the most recent developments in flash memory applications. The Summit consists of half-day tutorials, panel discussions, keynotes, presentation sessions, workshops, special sessions and exhibits.

Topics of Interest

- Design methods, best practices, emerging standards
- Consumer application requirements
- Flash software, controllers, and formats such as SD cards and USB drives
- Embedded applications
- Hybrid flash and HDD storage
- Storage security and programming requirements
- SDDs in computers, computer applications and flash-based microcontrollers

> "NAND flash has emerged as king of the memory jungle and now drives the memory process road map, a domain traditionally held by the DRAM."
> – Malcolm Penn, Future Horizons

Participating Companies include Intel, Samsung, SanDisk, Datalight, PNY, Kingston Memory, SST, STEC, Hagiwara, Smart Modular, Micron, Toshiba, Xiotech, Seagate and many more.

Sponsorship and Exhibiting Information:
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alan@flashmemorysummit.com

Who Should Attend?

- Designers of hardware, software, consumer electronics, memory and embedded systems
- Applications, storage, communications, computer,
- systems, and test engineers
- Storage specialists
- Engineering managers, systems analysts, solution providers and consultants
- VARs, OEMs, system integrators, venture capitalists, marketing and product managers

Keynote Speakers

- Ed Doller, IBM
- Jim Elliott, Samsung
- Eli Harari, SanDisk

Proposals for presentations are due by June 5

Please contact Lance Leventhal (+1-858-756-3327) with your proposed topic:
lance@flashmemorysummit.com

For more information, and to register online:

flashmemorysummit.com

IEEE SCV-CAS TUTORIAL

Broadband and RF Circuit Analysis and Design in CMOS Technology Part II

Saturday June 16, 2007 – 8:30 AM – 1:00 PM

at Cadence Design Systems – Bldg 5
2655 Seely Ave, San Jose

This tutorial, a continuation of the **Sept 2006** event, will familiarize engineering professionals with both classic and innovative new broadbanding techniques for CMOS technology amplifiers appropriate for state-of-the-art communication system applications, with a focus on **Distributed Amplifiers**. A unified circuit broadbanding strategy is discussed, as is a practical methodology for the monolithic realization of narrowband radio-frequency (RF) amplifiers. Because broadband and RF design necessarily entails the incorporation of suitable matching filters in signal flow paths, a reasonably extensive discussion of lossless filter architectures is incorporated in the tutorial. All theoretic and conceptual disclosures are verified through the results of realistic SPICE simulations.

Instructor: **Dr. John Choma**, Fellow, Scintera Networks, and Professor of EE & Systems Architecture Engineering, Univ of Southern California

Registration: 8:30 – 9:00 AM (includes pastries/coffee)
Sponsored lunch: 12:15 – 1:00 PM

Tutorial Outline:
9:00: "Introduction and Overview" by Dr. William Kao
9:15: "Tutorial Part III" by Dr. John Choma
10:45: "Tutorial Part IV" by Dr. John Choma

Topics: Overview of MOS Transistor Modeling; Noise Sources In NMOS and PMOS Devices; Gain and Bandwidth Optimization in Common Source Amplifiers; Broadband Architectures; Lossless Filters; Linearity Considerations

A CD of all lecture material and related notes will be provided to all attendees.

Registration Fee:
IEEE Member $40 Non-Member $50

Registration Deadline June 8 (postmarked by June 8)
After June 8 – if Space Available, $5.00 Surcharge

See full Tutorial Description for prerequisites and other details:

www.e-grid.net/docs/0705-scv-cas.pdf

Santa Clara University School of Engineering Graduate Programs

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Register by June 11
Students may continue to register until June 22.

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- IC Fabrication Processes - Optics Fundamentals
- Applied Mathematics - Logic Design Using HDL *(and more)*

Evening classes:
- Software Tools Design - Design Patterns
- Voice over IP - Electronic Circuits *(and more)*

Saturday classes:
- Mobile and Ad Hoc Networking - Law, Technology and Intellectual Property - Software Quality Assurance & Testing - Global Software Management *(and more)*

Choice of three Sessions:
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- Session II - 5-week classes (June 18 - July 20)
- Session III - 5-week classes (July 30 - August 31)

… plus a number of one-day Saturday classes

Email Wan Chen with inquiries: **WQChen@scu.edu**

To learn more, attend a Wednesday early-evening information session on **May 30** or **June 6**: Visit

www.scu.edu/engineering/graduate/rsvp.cfm

Review summer Open University courses:

www.scu.edu/ieee2

SCV Nanotechnology

TUESDAY May 29

Intellectual Property Strategy For Entrepreneurs, Technologists & Business Leaders

Speaker: David Mancino and Kevin Kirsch
Time: Registration & light lunch 11:30 AM; Presentation & Q/A 12:00 to 2:30 PM
Cost: none
Place: Silicon Valley Technical Institute, 1762 Technology Drive, suite #225, San Jose
RSVP: by email to KRS Murthy, drkrsmurthy@gmail.com

DAVID A. MANCINO is a Partner and Co-Chair of the Intellectual Property practice of Taft Stettinius & Hollister LLP. His technical background lies in Electrical Engineering and computer programming, and he has a Bachelor of Science in Electrical Engineering from the University of Michigan College of Engineering. Mr. Mancino, a registered patent attorney, litigates and prosecutes patents in many technical areas including: medical and surgical devices, prosthetics, software, business methods, electrical circuits, computer systems, computer networks, semiconductor device technology, jet engine technology, and many other mechanical and electro-mechanical technologies. He obtained his law degree from the University of Cincinnati School of Law in 1994 after working as a Senior Electrical Engineer for McDonnell Douglas Corporation.

KEVIN W. KIRSCH is a partner in the Cincinnati office of Taft, Stettinius & Hollister LLP. Mr. Kirsch is a peer reviewed AV Rated attorney who has represented companies in numerous complex commercial and intellectual property litigation matters. He is a patent attorney, licensed to practice before the United States Patent & Trademark Office. Mr. Kirsch recently testified before the United States House of Representatives, Committee on Small Business, at a March 29, 2007 hearing entitled, "The Importance of Patent Reform to Small Business." Mr. Kirsch received his undergraduate degree from the University of California at Berkeley and his law degree from Loyola Law School, Los Angeles.

Due to the enormous increase in patent application filings and patent infringement litigation suits in recent years, the importance of having a strategic plan with respect to patents is higher than ever. Speakers will discuss:

- Present patent and patent litigation landscape,
- Fluctuation of what is considered patentable subject matter by the US Patent Office,
- Many business purposes and uses for patents,
- Strategic considerations for a patent strategy,
- Common pitfalls dealing with patents both in-house and of the competition,
- Patent litigation considerations and costs,
- Recent trends in patent litigation, and
- Considerations in funding patent litigations

SCV Reliability

WEDNESDAY May 30

Designed Experiments and Reliability

Speaker: Ed Russell, National Semiconductor
Time: Refreshments at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: Oak room at HP, 19447 Pruneridge Avenue (Building 48), Cupertino
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/rl/events.htm

Ed Russell is a statistician at National Semiconductor in the SPICE Modeling group. He is currently working on analysis of electrical design rules and corner models, and is beginning implementation of statistical procedures for analog design. Prior to working at National, Ed was a statistician at Sun Microsystems where he developed and taught statistical procedures for 65nm and 45nm CMOS design. Before joining Sun, he served as the Director of Reliability for Cypress Semiconductors and, in addition, provided company wide statistical consulting with a general focus on test, product characterization, and process development for new technology. Ed also has held various management and individual contributor roles with AMD in both Austin and Sunnyvale working principally in reliability and yield improvement. While at AMD, Ed set up several SPC programs in the product lines, test, and logistics and served as the statistical programs manager at Sematech on assignment.

In addition to his role as a statistician in the semiconductor industry, Ed was Chevron's and Gulf Oil's expert in 3D signal processing, worked on evaluating the performance of the US High Level Nuclear Waste Repository, and has been heavily involved in software development and systems analysis. Ed received an MS degree in Mathematical Statistics from Purdue University with a concentration in Tests of Hypothesis and Decision Theory. After graduation, he continued his education with a focus on Biostatistics at the University of Washington, Multivariate Statistics at Ohio State, and Geophysics at The University of Houston.

Generally, the goal of a reliability analysis of lifetime data is to develop an estimate of how failures occur over time for a family of stress conditions. In either software or hardware reliability, experiments can be performed to determine if two or more alternatives (of e.g.: process, procedures, or design) may lead to significantly different reliability in a product. The speaker first presents a type of designed experiment for a very unusual setting -- choosing a procedural behavior among all possible procedural behaviors to optimize a general binary outcome to a 1 state (success or win) in the presence of multiple unknown countering procedures attempting to force a 0 state (failure or loss).

Initially, it's not at all clear that the subject is suitable for designed experiments of any kind due to extremely long runtimes, an environment which actively changes over time, and that there are typically between 2^{100} to 2^{3000} likely micro-behaviors at each stage of approximately 400 stages, most likely all correlated to some extent in both instance and across time, which may be considered the X's. To make matters even worse, the Y for which it is desired to optimize the behavior is not at all obvious. Should this setting be considered a reliability problem (failures do occur in time) or some other kind of experiment? The speaker shows how to cut through the muck and redefine the problem in a tractable manner.

The subject of the experiment is: How to win a "turns" based computer game -- at the highest level of the game -- in just 8 "runs" of the game. Given that a single game could take weeks to complete, 8 runs is very "expensive." Is it possible to reduce the "cost?" The concepts behind setting up a similar type of experiment with multiply censored data will be addressed and an analysis will be demonstrated. Finally, a few comments will be made on better methods for software and hardware design using statistical procedures.

SF Power Engineering

WEDNESDAY May 30

The Renaissance of Nuclear Power

Speakers: Professor Jasmina Vujic, Department of Nuclear Engineering, UC Berkeley, and Daniel Hirsch, lecturer in nuclear policy, UC Santa Cruz
Time: Social at 5:00 PM, dinner at 6:00 PM, Presentations and panel at 7:00 PM
Cost: $30 for IEEE members, $35 for non-members, $15 for Students (thru May 18)
Place: Monte Cristo Cafe. 4 Embarcadero Center, San Francisco (validated parking)
RSVP: reservation form to Jon Eric Thalman, jetg@pge.com
Web: www.ewh.ieee.org/r6/san_francisco/pes

With growing concern about increasing carbon emissions and the potential for global warming, interest is increasing in the development of nuclear power as a source of carbon-free electrical energy. We have invited two experts in the field to share disparate insights and perspectives about the future of nuclear power in California and the nation.

Please download the registration and meal selection form from the website and make your payment prior to the dinner.

Professor Jasmina Vujic is Chair of the Department of Nuclear Engineering at UC Berkeley. She teaches undergraduate courses in nuclear engineering, nuclear reactor theory, and radiation protection and control; as well as graduate courses in nuclear reactor theory and numerical methods in reactor design and analysis. Her research interests include methods for the neutronic analysis of nuclear reactors, radiation shielding, and medical applications of radiation; neutron and photon transport theory; and reactor core design and analysis.

Daniel Hirsch is a lecturer in nuclear policy at the University of California, Santa Cruz, where he founded and was the first Director of the Stevenson Program on Nuclear Policy. He is also President of the Committee to Bridge the Gap, a 37-year-old non-profit public policy organization focused on issues of nuclear safety, waste disposal, proliferation, and disarmament.

SF Engineering in Medicine and Biology

WEDNESDAY May 30

Physiological MR Imaging and Spectroscopy of Brain Tumors

Speaker: Dr. Tracy Richmond McKnight, Assistant Professor of Radiology, UCSF
Time: Social at 6:00 PM, dinner at 7:00 PM
Cost: $15 for IEEE members, $25 for non-members, $10 for Students (thru May 25)
Place: Sinbad's Pier 2 Restaurant, Pier 2 Embarcadero St., SF
RSVP: reserve by email with Bob Giebeler, b.giebeler@ieee.org or 415-252-7214
Web: www.e-grid.net/docs/0705-sf-emb.pdf

Our presenter, **Dr. Tracy Richmond McKnight** is currently an Assistant Professor in the Department of Radiology at the University of California, San Francisco (UCSF). She is a member of the UCSF Brain Tumor Research Center, the UCSF Comprehensive Cancer Center, and the UCSF/UCB Joint Bioengineering Graduate Group. Dr. McKnight received her B.S. degree in physics from Spelman College in Atlanta, GA, her M.S. degree in physics from Polytechnic University in Brooklyn, NY, and a PhD in Bioengineering from the University of California, Davis.

The primary goal of Dr. McKnight's research program is to investigate the malignant progression of brain tumors using techniques that can be incorporated into clinical diagnostic and patient management strategies. Her current approach is to correlate in vivo physiological magnetic resonance imaging (MRI) and spectroscopic (MRS) features of human brain tumors with ex vivo measures of molecular alterations associated with tumor aggressiveness. The expectation is that early molecular events that do not cause a change in tissue morphology, and are therefore invisible on conventional MRI, will exhibit a chemical signal that is distinct from surrounding normal tissue and can be detected with physiological MRI/MRS methods.

SCV Computer

SATURDAY June 2

Multicore: the New Face of Computing -- Promises and Challenges

Speakers: Professors and practitioners
Time: Registration at 8:30 AM; program from 9:00 AM - 4:30 PM
Cost: $45 for IEEE members, $55 for non-members, $25 for Students, higher on-site (includes lunch)
Place: Stanford's Braum Auditorium
RSVP: please reserve on the website
Web: www.natea.org/sv/conferences/nfic/2007/nfic_2007.php

This joint IEEE-NATEA conference on an emerging technology is aimed to provide IEEE and NATEA members with an inexpensive but solid overview of a technology that may affect their work and careers in the near future. This annual Saturday conference series has been traditionally held at Stanford on a Saturday. This year the date is June 2nd at the Bio-X facility or Braun Auditorium (TBD). Over the past 8 years we have covered such topics as RFID, SOC, Bioinformatics and Nanotechnology.

With the advent of the Sony PS3 and its utilization of a powerful multicore technology, new opportunities for other non-game scientific and technology applications present themselves. To date there has been some appreciation of this new and significant change in high-end computation. Utilization in such research as protein folding has been suggested. This conference seeks to summarize where this technology stands and what issues must be addressed to bring the exciting and powerful world of multicore computing to fruition in the scientific and technical communities to unleash its promise.

The conference will present a technical overview of the hardware and software issues involved in this significant change in computing including such issues as compilation, scalability graphics co-processing and potential applications in the scientific domain.

See the website for the full program, or contact Dale Gutierrez at dalegut@aol.com.

SCV Professional Activities Committee for Engineers (PACE)

MONDAY June 4

Who Wants to be a Start-Up Star? (... and What it Takes)

Speakers:	A panel of folks who have built successful startups
Time:	Dinner (optional) 6:30 PM; Panel at 7:30 PM
Cost:	$10 plus beverages for optional dinner; no cost for panel
Place:	India Grand Buffet, 1214 Apollo Way, Sunnyvale
RSVP:	not required
Web:	ieee-jbdavid.blogspot.com/

Please join us on Monday, June 4th for this exciting discussion. Check the website for Bio's of our Panelists.

Silicon Valley is still a GREAT place for startups to form.. Here we have great research universities to generate ideas, Venture Capital firms for seed money, and the greatest concentration of technical talent. Yet one of the challenges startups face is finding and hiring the RIGHT talent.

From our point of view, as potential startup employee's, we'd like to know how to get to be that Talent.

We have assembled a panel of folks who have built successful startups, to discuss what they look for in their early hires. Questions to be discussed include:

- What are the essential qualities that differentiate the successful employees they would hire for their next startup from those who have great talent, but shouldn't be hired in a startup situation?
- How should startup candidates prepare for their interview?
- What kinds of experiences show those qualities?
- When we are available, how do we get "in the loop" to learn about potential startups?

SCV Lasers and Electro Optics

TUESDAY June 5

Progress in Reliable High-Power Diode Lasers: Near-infrared Diode Lasers and Applications

Speaker: Toby Strite, Manager, High Power Laser Marketing, JDSU
Time: Networking and Pizza at 7:00 PM; Presentation at 8:00 PM
Cost: none
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/leos

Details about the LEOS Meeting were not available as the GRID went to press. Please check the LEOS Chapter web page.

Thri-Section GOLD - Grads Of the Last Decade

SATURDAY June 9

Tri-Section GOLD Networking Event: Breakfast and Networking

Speakers: A panel of experienced engineers and managers
Time: Complimentary breakfast at 8:30 AM, Networking with real-world tips for your career from 9:30 - 11:30 AM
Cost: none
Place: Michael's at Shoreline, 2960 N. Shoreline Blvd., Mountain View
RSVP: by email to Bill DeHope, dehope1@llnl.gov

Peter Tarver took his new BSEE from CSU

All Engineers who graduated from university since 1997 (give or take a few years!) are invited to a free breakfast and networking event. Details:

- 8:30 AM Hosted Breakfast Buffet
- 9:30-11:30 Networking Event
- at Michael's at Shoreline
- 2960 N. Shoreline Blvd., Mountain View
(Exit Shoreline North off 101)

This event for our "Grads Of the Last Decade" (GOLD) is sponsored by the San Francisco Bay Area Council. It will be a loosely structured format that ensures that you leave with real-world tips that will help you in growing your career. There is no cost to you -- but you must register in advance. Information requests and RSVPs to: Bill DeHope, dehope1@llnl.gov

See also the **hike in San Francisco** on July 15th!

SCV Magnetics

TUESDAY June 12

Long Data Sectors, Capacity Growth and Data Integrity in HDD's

Speaker: Martin Hassner, Hitachi Global Storage Technologies
Time: Cookies and drinks at 7:30 PM; Presentation at 8:00 PM
Cost: none
Place: KOMAG, 1710 Automation Parkway, San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/mag

The continued growth of HDD Capacity, at the current 512-Byte fixed Sector Format, is incompatible with the Storage User requirement of simultaneously improving the Data Integrity. The consequence of these incompatible requirements is a bottleneck that seems to limit the HDD industry's capacity growth. Long Data Sector coding solutions that resolve this bottleneck will be discussed.

Martin Hassner received a B.Sc and M.Sc at the Technion, Israel, and a Ph.D in 1980 at UCLA, all in Electrical Engineering. In 1980 he joined the IBM Research Division and has since worked on Coding and Signal Processing Applications for Magnetic Recording. Since 2002, when the IBM Storage Division and Research part were acquired by HITACHI, he has been with Hitachi GST Research.

Applications of his UCLA Ph.D. thesis on Modulation Codes, specifically the (1,7)-Code application, have been widely used throughout the industry during the 80's. The paper describing his Ph.D thesis work was also awarded the Best Paper Award by the IEEE Transactions on Information Theory in 1986. In 1990 he introduced the first Key Equation Solver Reed Solomon-Decoder implementation in a Hard Disk Controller in IBM Storage Products. He has received several IBM Outstanding Innovation Awards and was an IBM Master Inventor. He holds 50 US Patents.

WEDNESDAY June 13

uPILR MicroContacts: A Next-Generation Chip-Scale Packaging Solution

Speaker: Dr. Belgacem Haba, Tessera, Inc.
Time: 6:30 PM dinner (optional); 7:30 PM Presentation
Cost: Seated dinner served at 6:30 - $25 if reserved by June 11; $30 after & at door
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road near Lawrence Expy), Sunnyvale
RSVP: through PayPal on website, or by email to Janis Karklins, karklins@ieee.org
Web: www.cpmt.org/scv

Dr. Bel Haba joined Tessera as a Fellow in October 2002 and became CTO of Advanced Packaging and Interconnect in April 2006. He is responsible for overseeing next-generation research and development activities for Tessera, Inc. Dr. Haba is also a founder of SiliconPipe Inc., a high-speed interconnect start-up company based in Silicon Valley. Prior to that, he managed the packaging research and development division at Rambus. From 1991 to 1996, he managed advanced research and development projects at the NEC Central Research Laboratories in Japan and, prior to that, worked for IBM at its T.J. Watson Research Center in New York. During his tenure at NEC and IBM, Dr. Haba's activities included the applications of lasers in the field of microelectronics.

Dr. Haba received his bachelor's degree in solid state physics from the University of Bab-Ezouar, Algeria in 1980. He holds two master's degrees in applied physics, materials science and engineering from Stanford University, where he also earned a Ph.D. in materials science and engineering in 1988. Dr. Haba holds 85 U.S. patents, and over 130 worldwide patents and patent applications. He has authored numerous technical publications and has also participated in many conferences worldwide

Hand-held communication and entertainment products will continue to dominate the consumer markets worldwide and, with each generation offering more and more features and/or capability, system level integration and miniaturization becomes more of a priority. And even though the actual applications and functionality of the new product offering expands, the customer is expecting each generation to be smaller and lighter that its predecessor. A number of single-die and stacked-die package innovations have been developed for this broad market but many supplier companies are not meeting acceptable manufacturing yields and the difficulty of simultaneous testing of multiple mixed-die technology is not always practical. Without implementing more innovative package methods, the functional capability of the newer generation of hand-held and portable products may never reach expectation or achieve manufacturing cost objectives.

The challenge manufacturers face when competing in the world marketplace is to offer a product that will meet all performance and functionality expectations without increasing product size or cost. Increased electronic functionality can be achieved through the development of more complex silicon integration but that route generally requires a great deal of capital resources and an excessive amount of time. Multiple-die package concepts are often proving superior to the system-on-chip alternative because it minimizes risk and has the potential for economically integrating several different but complementary functions. The information presented in this paper will review several package-on-package configurations and introduce a new packaging technology. A non-solder ball package, called "MicroContact", is based on a new substrate fabrication process developed to improve IC package density and circuit routing efficiency. In addition, the basic MicroContact package assembly methodology will be described and examples of high density stacked memory and mixed function variations shown. We will discuss the MicroContact effect on pitch, socketless testing, low profile, and reliability especially on lead free drop test.

SCV Consumer Electronics

TUESDAY June 19

Biometrics: Finger Print Sensor Technology

Speaker: Jalil Shaikh, Chief Executive Officer, Validity Sensors, Inc.
Time: Pizza and drinks at 6:30 PM; Presentation at 7:00 PM
Cost: $5 for members, $10 for non-members
Place: Oak room at HP, 19447 Pruneridge Avenue (Building 48), Cupertino
RSVP: not required
Web: ewh.ieee.org/r6/scv/ce

Biometric security is quickly becoming a reality. However, within Biometrics, Finger Print Sensors (FPS) are the most cost-effective solution. Currently, FPS is mostly popular in laptop computers for its ease of use for password replacement.

Validity has developed a unique, patented, rugged and cost effective FPS technology which is quickly becoming popular in the market place.

Jalil Shaikh is the Chief Executive Officer at Validity. Mr. Shaikh was most recently a VP & Assistant GM at Broadcom following their successful acquisition of Zeevo, Inc. in 2005. As President and CEO of Zeevo, he led a resurgence of the company to exponential revenue growth and substantial cost reductions, while defining new market opportunities for Zeevo Bluetooth stereo audio products. Prior to Zeevo, as EVP of Operations, Mr. Shaikh, as a very early employee, was a key contributor to Silicon Image's rapid growth and eventual successful IPO. He was also significant factor in the growth and success of Trident Systems, Micro Linear and Matra Design Semiconductor. At National Semiconductor he was with the MOS Analog group which enjoyed extremely rapid revenue growth during his four year tenure.

SCV Nanotechnology

TUESDAY June 19

Polymer Nanocomposites: Fabrication, Characterization and Application

Speaker: Dr. W. Richard Chung, Professor, Department of Chemical and Materials Engineering, San Jose State University
Time: Registration & light lunch 11:30 AM. Presentation at 12:00 Noon
Cost: IEEE Members and Students $5. Non-Members $10
Place: SEMI World Headquarters 3081 Zanker Rd. San Jose
RSVP: on our web site: www.ieee.org/nano
Web: www.ieee.org/nano

Dr. W. Richard Chung is Professor of Chemical and Materials Engineering at San Jose State University. He has taught courses and conducted research projects at SJSU for 20 years. Prior to joining the faculty of SJSU, he also worked as an engineer in various industries, i.e. paper and pulp, plastics manufacturing, and nuclear power plant design and construction. His research interests concentrate on intelligent materials, nanocomposites, polymers and composites, product design and process control, and failure analysis. He received a Hall of Fame Award, Golden Gate Section, Society of Plastics Engineers (2001), a Service Award, Faculty Leadership Institute, Workforce Silicon Valley (2001), an Appreciation Award, Lockheed Martin Space and Missiles Corporation (2002), and an Outstanding Alumni Award, Auburn University (2002).

Nanocomposite materials are defined as two-phase materials with one phase having at least one dimension on the nanometer scale. These materials have sparked an interest in research and development for various engineering and industrial applications. Some notable applications include gas separation, fuel cell membrane development, heat shielding, food packaging, sensing and actuating, and microelectronic applications. Nanocomposites can be manufactured using polymeric or non-polymeric resins as the matrices. To limit the scope of this presentation, only polymer nanocomposites are to be employed, i.e. polymer resins are to be filled with nanometer sized inorganic particles. Processing techniques with material variables such as volume fraction, nanoclay type (modified and unmodified), polymer type, pore size and pore density will be addressed. Their inter-relationships among material properties and processing techniques will be examined along with various characterization methods. Among these, the results of x-ray diffraction, X-ray reflectivity, scanning/transmission electron microscopy and atomic force microscopy will be presented and discussed. The results of this presentation will shed some light on the development of future nanocomposites

WEDNESDAY June 20

Bionic Technology for Mobility Assistance

Speaker: Robert Horst, Ph.D., Chief Technology Officer, Tibion Corporation
Time: optional dinner with the speaker, Stanford Hospital cafeteria, at 6:15 PM; Presentation at 7:30 PM
Cost: none
Place: Clark Center Auditorium, Stanford Univ (free parking after 4 PM)
RSVP: not required
Web: www.ieee.org/scv/embs

Robert Horst is Chief Technology Officer at Tibion Corporation, a company he co-founded in 2002. He holds an BSEE degree from Bradley University, a MSEE from the University of Illinois at Urbana-Champaign, and a Ph.D. in computer science also from the University of Illinois. He is a Fellow of the IEEE and holds 65 US patents.

Powered mobility assistance devices, sometimes called active orthotics, bionics, bio-robotics, or exoskeletons, could have a tremendous impact on the quality of life for those with impaired mobility. Advances in embedded computing, lightweight batteries, and motor control electronics provide some of the needed technologies, but the field has developed slowly while waiting for a suitable actuator that meets all of the key requirements: 1) Strong enough to lift a person, 2) Small and light enough to fit under the clothing 3) Coupling/gearing to provide a range of speed/torque tradeoffs as well as free movement, and 4) Highly efficient operation to power the device for a full day with a small battery.

Tibion has been developing actuators, electronics and embedded software to address the requirements for active orthotic devices. The development has included fabrication and testing of many types of actuators to deliver the required forces while minimizing size and weight. The evolution of the design requirements and solutions will be presented through photos, video and analysis of this series of prototypes. These devices are based on new types of continuously variable transmissions (CVTs) that provide the variable impedance needed for bionic applications. The actuators deliver sufficient force to aid in rising from a chair, the ability to deliver assistance force while moving quickly, and unimpeded motion during the swing phase of the gait. The discussion will include many aspects of developing an active knee device using a CVT actuator.

OEB Industry Applications

THURSDAY June 21

So what's Wrong with your Data Center or UPS Designs?

Speaker: Glyn J. Lewis, Applied Power
Time: No-host social at 5:30 PM; Presentation at 6:15 PM; Dinner at 7:15 PM Presentation continues at 8:00 PM
Cost: $20 for IEEE members; $25 for non-members
Place: Marie Callender's Restaurant - The Garden Room; 2090 Diamond Blvd, Concord (near Concord Hilton Hotel)
RSVP: Please make reservations by June 20, by contacting Gregg Boltz at gboltz@brwncald.com or telephone (925) 210-2571
Web: www.e-grid.net/docs/0706-oeb-ias.pdf

Glyn J. Lewis graduated from the University of Wales Institute of Science and Technology in 1964. He worked for two switchgear suppliers in UK as a commissioning engineer. In 1968, he joined GE and worked in several positions until forming Applied Power in 1981.

Mr. Lewis has performed over 500 analytical studies on electrical distribution systems in the areas of short circuit analysis, coordination, load flow and motor starting. He is responsible for the design of numerous generating and cogeneration plants and specializes in the design of high voltage systems and controls utilizing the latest technology devices.

Mr. Lewis was the principle instructor for many training seminars presented by General Electric Company in the fields of electrical safety, switchgear, and protective relaying. He was selected by IEEE as an instructor in the San Francisco short course on high voltage substation design. He was also selected by IEEE as an instructor in the 1984, 1985, 1987, 1991, 1993 and 1994 to conduct the San Francisco and Los Angeles, Industry Applications Society's and the Power Engineering Society's short courses on fault calculations and coordination studies.

Mr. Lewis is a member of IEEE, NFPA, NETA, IAEI and ASE, and registered in the State of California.

The June 21st meeting of the Industry Applications Society for Oakland East Bay Section will feature a talk entitled "So what's wrong with your data center or UPS designs?". The speaker will be Glyn J. Lewis, Applied Power.

Numerous data centers and UPS systems are inherently going to fail due to the wrong selection of hardware by the designers and the manufacturers. This brief talk will point out the common deficiencies in the design, and addresses the solutions from a system standpoint. The words "failure" or "faults" do not seem to appear in the data center personnel's vocabulary whether they are designing, supplying or operating systems with UPS modules. Most systems are designed around the load requirements in N+1 or N+2 configurations. However, the designs do not take into account the N+1 or N+2 requirements under fault conditions.

Glyn Lewis of Applied Power has designed several data centers and analyzed numerous UPS systems in the performance of over 500 short circuit and coordination studies. This presentation will offer common designs used in data centers and point out the pros and cons of each design. There will also be a discussion about actual case histories that have caused complete loss of a data center or UPS system.

SCV Power Safety Engineering

TUESDAY June 26

Telecomm Topics – FAQs (and Answers)

Speaker: Peter Tarver, Sanmina-SCI Corporation
Time: Optional dinner at El Torito at 5:45 PM; Presentation at Applied Materials at 7:00 PM
Cost: Optional dinner (no-host); no cost for presentation
Place: Dinner at El Torito Mexican Restaurant, 2950 Lakeside Drive, Santa Clara; presentation at Applied Materials, Bowers Café, 3090 Bowers Ave, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/pses

Tonight's speaker starts with the basics – "What is TNV?" – but doesn't stop there. Topics include:

- How do I know if my interface is TNV-x?
- What's so hazardous about that?
- What about Power over Ethernet (PoE)?
- What level of insulation do I need?
- What's this I hear about Nordic countries?
  - What special tests do I need to perform?
- Does having a TNV circuit in my product affect otherwise required tests?
- Can I get around any of that?
- Introduction to Remote Power Feeding (if time allows).

Peter Tarver took his new BSEE from CSU Fresno to Underwriters Laboratories in 1984. He obtained his Professional Engineer License in 1987. By 1989 Peter was the Designated Engineer at UL's Santa Clara office for all telephone and related equipment product categories.

In 1994 Peter joined Northern Telecom (now called Nortel Networks). He worked primarily on their flagship enterprise level PBX product and ancillary equipment, as well as voice messaging and call server equipment. Peter moved to Sanmina-SCI Corporation, a contract manufacturing company, in 2000, where he provides product safety consulting, testing and agency liaison services.

Peter is a member of IEEE PSES; CSA/UL Bi-National Working Group for 60950-1; UL Standards Technical Panel 60950, Information Technology and Telecommunication Equipment; Telecommunication Industry Association Technical Committee on Environmental and Safety Considerations, TR41.7 and various subcommittees.

Monterey Bay Subsection

THURSDAY June 28

Exploring the Ocean Using Autonomous Underwater Vehicles

Speaker: Dr. Yanwu Zhang, Monterey Bay Aquarium Research Institute
Time: Refreshments, food at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: Business With Pleasure, 216G Mt. Hermon Rd., Scotts Valley
RSVP: via email to Marcelo Siero, siero@ee.com
Web: www.ee.com/auv

Yanwu Zhang (S'95-M'00-SM'05) was born in 1969 in Shaanxi Province, China. He received the B.S. degree in Electrical Engineering and the M.S. degree in Underwater Acoustics Engineering from Northwestern Polytechnic University, Xi'an, China, in 1989 and 1991, respectively. In 1998, he received the M.S. degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology (MIT). In June 2000, he received the Ph.D. degree in Oceanographic Engineering from the MIT/Woods Hole Oceanographic Institution (WHOI) Joint Program.

From June to December 2000, Dr. Zhang was a Systems Engineer working on medical image processing at the General Electric Company Research and Development Center, Niskayuna, NY. From January 2001 to November 2004, he was a Digital Signal Processing (DSP) Engineer and then promoted to a Senior DSP Engineer at Aware Inc., Bedford, MA, working on digital communications. Since December 2004, he has been with the Monterey Bay Aquarium Research Institute, as a Senior Research Specialist engaged in Autonomous Underwater Vehicles (AUVs) and ocean observing systems. Dr. Zhang's current research interests are mainly in spatio-temporal signal processing and its applications to AUVs' sampling of oceanographic processes. He has had papers published in IEEE Journal of Oceanic Engineering, IEEE Transactions on Signal Processing, IEEE Transactions on Neural Networks, Journal of Atmospheric and Oceanic Technology, and conference proceedings. He also served as a reviewer for academic journals, as well as for National Science Foundation (NSF) and National Oceanic and Atmospheric Administration (NOAA) proposals. He is the author of "Chapter 11: Complex-Valued Generalized Hebbian Algorithm and Its Applications to Sensor Array Signal Processing" in Complex-Valued Neural Networks: Theories and Applications, published by the World Scientific Publishing Co. in 2003. Dr. Zhang is a Senior Member of IEEE, and a member of Sigma Xi. He was a finalist for MIT Technology Review Magazine's 100 young innovators (TR100) in 1999.

Exploring the ocean is a difficult task due to the oceans' vastness, depth, variabilities, and often hostile conditions. The Monterey Bay Aquarium Research Institute (MBARI) has been developing autonomous underwater vehicles (AUVs) and deep-sea networks to revolutionize the observation of the ocean's interior. In this talk, Dr. Yanwu Zhang will introduce MBARI's Dorado-class AUVs in the context of the Autonomous Ocean Sampling Network (AOSN). He will show the AUV's architecture and various sensors. The fundamental challenge of ocean observation is that ocean processes vary both spatially and temporally. With agility and speed, AUVs bring about new capabilities to resolve the spatio-temporal variability. In this talk, Dr. Zhang will discuss how to take advantage of different categories of autonomous platforms to optimally measure the ocean. He will show some results from AUV experiments in the Monterey Bay. MBARI's current development of AUV docking and longer-range AUVs will enhance the vehicles' capabilities and further incorporate them into the ocean observatory system.

SCV Solid State Circuits

THURSDAY June 28

First Time, Every Time: Practical Advice for Phase-Locked Loop Design Success in a Modern CMOS World

Speaker: Dennis Fischette, AMD
Time: Refreshments, food at 6:00 PM; Presentation at 6:30 PM
Cost: Donation requested to partially cover food cost
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Dr., Santa Clara
RSVP: via email to ssc_scv_rsvp@yahoogroups.com
Web: www.ewh.ieee.org/r6/scv/ssc

Dennis Fischette designs mixed-signal circuits at Advanced Micro Devices in Sunnyvale, CA. His technical interests include PLL and DLL design, clock-and-data recovery, circuit analysis software, and high-speed IO circuits. He is a member of the IEEE Distinguished Lecturer program as well as the CICC Technical Program Committee. He was a member of the ISSCC Technical Program Committee from 2001-2006.

He graduated from Cornell University, Ithaca, NY, with Physics BSc in 1986. Before seeking fame and fortune in Silicon Valley, he pursued graduate studies in the History of Science at the University of California, Berkeley.

Dennis is known to "toot his own horn" all over the SF Bay Area as a trombonist with several jazz ensembles. He recently toured China and Vietnam with the SFBayJazz big band.

The phase-locked loop (PLL) is an often feared and misunderstood beast. Black-box designs from IP vendors are integrated on-chip with little understanding of the PLL's sensitivities to process and digital noise. Inexperienced designers read the latest literature and try to hit a "home run" with their first PLL. Ignorance of the PLL's internal workings leads to impossible-to-meet specs and inadequate test features. The result? Costly silicon spins, hapless debug efforts, and missed product windows.

This presentation provides a practical exploration of real-world PLL design for clock generation and high-speed IO (e.g. PCI-Express) with emphasis on 45nm and 65nm designs. Topics include

- achieving a real physical feel for feedback stability
- common circuit implementations and how they can go horribly wrong
- avoiding late nights in the lab with inexpensive test and debug features
- defining, isolating, and measuring PLL jitter
- creating a tape-out checklist to ensure first-pass success
- subtle design implications of high-speed IO clocks
- real-world failures and successes.

SF Grads Of the Last Decade (GOLD)

SUNDAY July 15

IEEE GOLD Networking Event & Hike at Land's End

Event:	Come explore the SF coast and the Cliff House nearby.
Time:	2:00 PM
Cost:	none
Place:	parking lot at Point Lobos Ave. and Merrie Way, SF
RSVP:	by email to ahammer@ieee.org
Web:	Alex Goldhammer, ahammer@ieee.org

Come explore the beauty of the San Francisco coast while meeting up with fellow IEEE Graduates Of the Last Decade (GOLD). We'll spend some time after the hike at the Cliff House nearby.

Send email to Alex Goldhammer for details!

SCV Consumer Electronics

TUESDAY July 24

DisplaySearch Projections for HDTV

Speaker:	Paul Gagnon, Director of North American TV Research, DisplaySearch
Time:	Pizza and drinks at 6:30 PM; Presentation at 7:00 PM
Cost:	$5 for members, $10 for non-members
Place:	Oak room at HP, 19447 Pruneridge Avenue (Building 48), Cupertino
RSVP:	not required
Web:	ewh.ieee.org/r6/scv/ce

Paul Gagnon is Director of North American TV Research. Paul has 10 years of experience in the Consumer Electronics industry, both on the retail and manufacturing side, adding value and insight to DisplaySearch's industry leading analysis. He most recently worked as Sr. Marketing Analyst for Hitachi America LTD's Home Electronics Division, forecasting and analyzing volatile TV and Video market trends. His responsibilities included weekly and monthly market analysis, competitive information tracking and extensive involvement in product and strategic planning. He was also responsible for developing and implementing retail sales incentive promotions. In addition, Mr. Gagnon was a member of the CEA Video Division Market Research Committee.

The speaker will cover the current state of the HDTV market, new directions in technology development and the latest global TV shipments and forecasts.

SCV Consumer Electronics

TUESDAY August 28

WirelessHD: High Bandwidth for Home Entertainment

Speaker: John Marshall, President, Wireless High Definition (WirelessHD) Consortium
Time: Pizza and drinks at 6:30 PM; Presentation at 7:00 PM
Cost: $5 for members, $10 for non-members
Place: Oak room at HP, 19447 Pruneridge Avenue (Building 48), Cupertino
RSVP: not required
Web: ewh.ieee.org/r6/scv/ce

John Marshall is President of the Wireless High Definition (WirelessHD) Consortium and President of WirelessHD, LLC, an organization comprising the world's leading consumer electronics companies, including LGE, NEC, Panasonic, Sony, Samsung, Toshiba. The Group is revolutionizing the home entertainment experience by enabling wireless, uncompressed sharing of high definition content among a wide range of home entertainment components (HDTVs, DVD players, et al.) and HD imaging devices (digital video and still cameras, et al.).

Marshall is also Vice President of Marketing for SiBEAM, Inc. Bringing ten years leadership of startup and Fortune 500 business operations, Marshall is responsible for SiBEAM's product and market vision and manages marketing, business development and sales. Since SiBEAM's inception, Marshall also led the formation of the WirelessHD™ special interest group focusing on A/V networking and currently serves as the president of WirelessHD, LLC.

Prior to joining SiBEAM, Marshall served as vice president of marketing and business development at 2Wire, Inc., a leading broadband services platform developer, supporting its growth from first product to market leadership on over $150M in worldwide revenue. Prior to 2Wire, Marshall co-founded 3Com's Wireless & Home Networking Division, capturing market leadership for its first product line in its first year. At 3Com prior, Marshall led emerging market development in ICE markets (information, communications, entertainment) from $40M to $400M revenue.

Prior to 3Com, Marshall worked for a marketing consultancy advising technology companies on market entry strategy, segmentation, pricing, and competitive analysis. In addition to his work at SiBEAM, Marshall has served on the advisory board of Ruckus Wireless, as president of the Home Phoneline Networking Alliance (HomePNA), the board of USC's Entertainment Technology Center (ETC) and the Association for Interactive Media (AIM).

Marshall holds a B.A. from Northwestern University and MBA from the University of Michigan's Ross School of Business.

SCV Magnetics

TUESDAY September 15

State-of-the-art Ferrite Materials for Fundamental Research, Nano-science, and High-Frequency Applications

Speaker:	Prof. Vince Harris, Northeastern University, Boston
Time:	Cookies and drinks at 7:30 PM; Presentation at 8:00 PM
Cost:	none
Place:	KOMAG, 1710 Automation Parkway, San Jose
RSVP:	not required
Web:	www.ewh.ieee.org/r6/scv/mag

Prof. Vincent G. Harris received the B.Sc., M.Sc., and Ph.D. (1990) degrees in engineering from Northeastern University. He has also received the M.Sc. degree in engineering management from the University of Maryland (1995), and the M.Sc. degree in executive technology management from the Wharton School at University of Pennsylvania (2003). He is presently the William Lincoln Smith Chair Professor in the Electrical and Computer Engineering Department at Northeastern University.

Dr. Harris was a member of the technical staff at the Naval Research Laboratory (1990-2003). During his time at NRL he served as the head of the Complex Materials Section and the head of the Materials Physics Branch. In 2001 he established and assumed the position of director of the NRL Synchrotron Radiation Consortium. In 2004 he established the Center for Microwave and Magnetic Materials and Integrated Circuits, and continues to serve as its first director . The mission of this center is to develop high frequency materials and device solutions for next-generation radar and wireless communication electronics.

His research interests include materials design and the study of processing, structure, and magnetism in a wide range of materials. He has pioneered the use of synchrotron radiation techniques to relate the short range chemical and structural properties of materials to magnetism. He has published more than 170 technical articles, including book chapters and review articles on the topical areas of nanotechnology, magnetism, and magnetic materials. In addition, he holds nine patents and patent applications, and has presented more than 150 papers at national and international meetings. Dr. Harris is a Fellow of the American Physical Society and Senior Member of the IEEE.

Ferrite materials have long played an important role in power conditioning, conversion, and generation across a wide spectrum of frequencies (up to 10 decades). They remain the preferred magnetic materials, having suitably low losses, for most applications above 1 MHz, and are the only viable materials for nonreciprocal magnetic microwave and millimeter wave devices (including tunable filters, isolators, phase shifters, and circulators). Recently, novel processing techniques have lead to a resurgence of research interest in the design and processing of ferrite materials as nanoparticles, films, single crystals, and metamaterials. These latest developments have set the stage for their use in emerging technologies that include cancer remediation therapies such as magneto-hyperthermia, magnetic targeted drug delivery, and magneto-rheological fluids, as well as enhanced magnetic resonance imaging.

With reduced dimensionality of nanoparticles and films, and the inherent nonequilibrium nature of many processing schemes, changes in local chemistry and structure have profound effects on the functional properties and performance of ferrites. In this lecture, we will explore these effects upon the fundamental magnetic and electronic properties of ferrites. Density functional theory will be applied to predict the properties of these ferrites, with synchrotron radiation techniques used to elucidate the chemical and structural short-range order. This approach will be extended to study the atomic design of ferrites by alternating target laser-ablation deposition. Recently, this approach has been shown to produce ferrites that offer attractive properties not found in conventionally grown ferrites. We will explore the latest research developments involving ferrites as related to microwave and millimeter wave applications and the attempt to integrate these materials with semiconductor materials platforms.